vCXLGen

Automated Synthesis and Verification of CXL Bridges for Heterogeneous Architectures

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Heterogeneous compute in modern data centers

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- **Increasing CPU diversity:**

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Major players develop their own silicon

Building scalable data centers

With resource disaggregation

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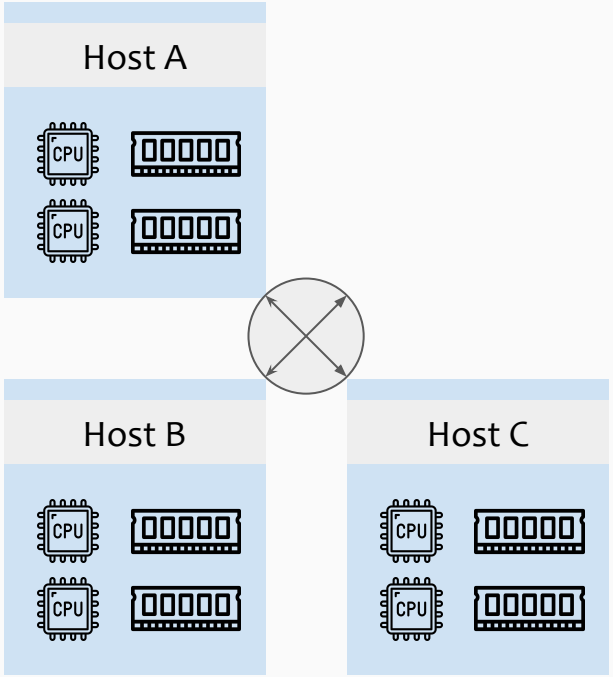

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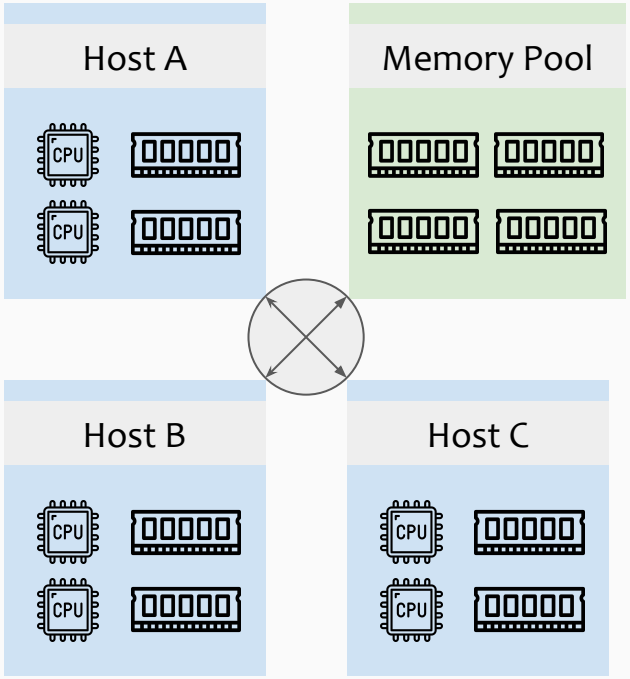

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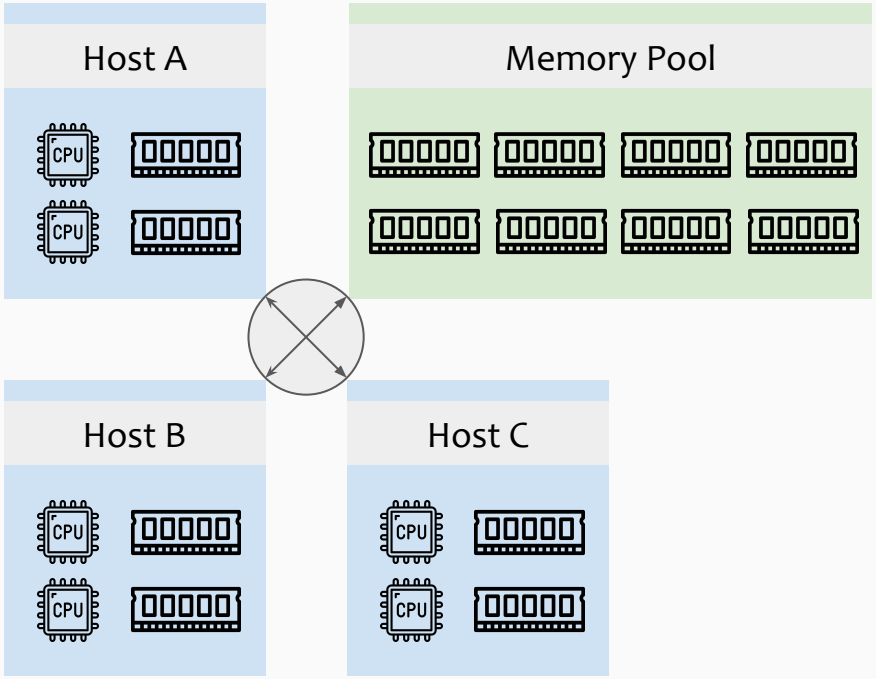

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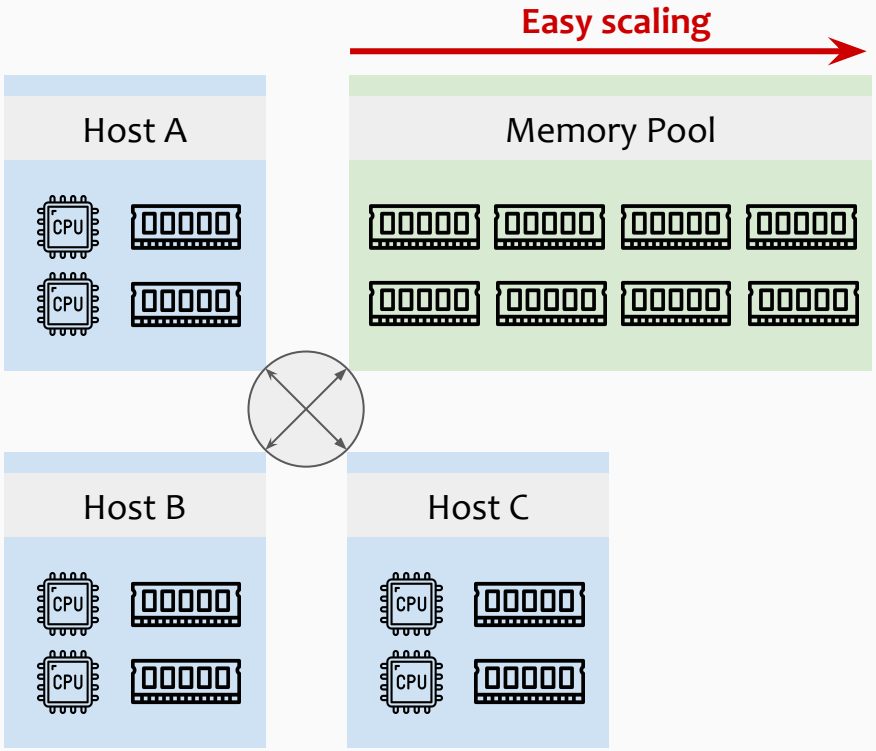

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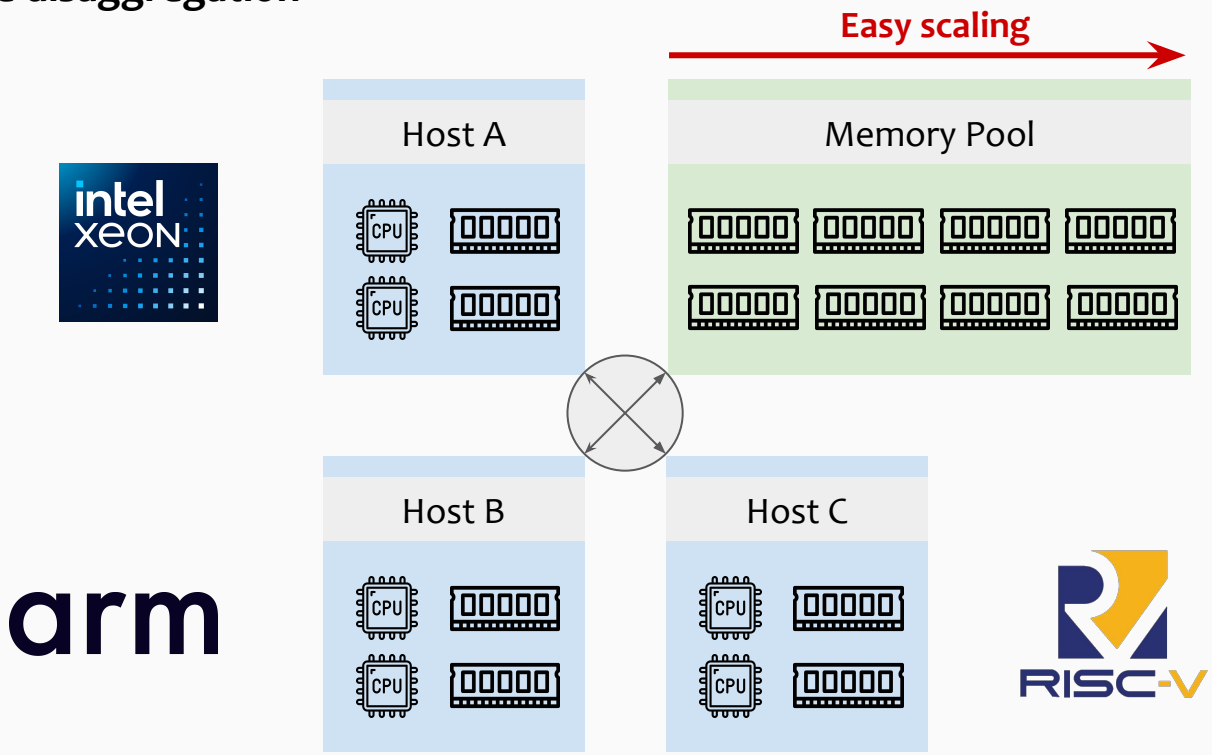

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  - Implemented in hardware
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Can CXL compose **heterogeneous architectures ?**

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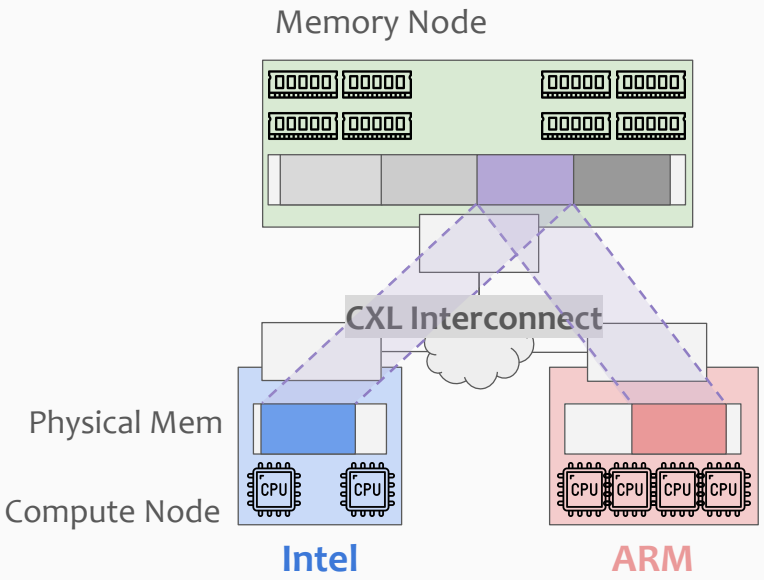

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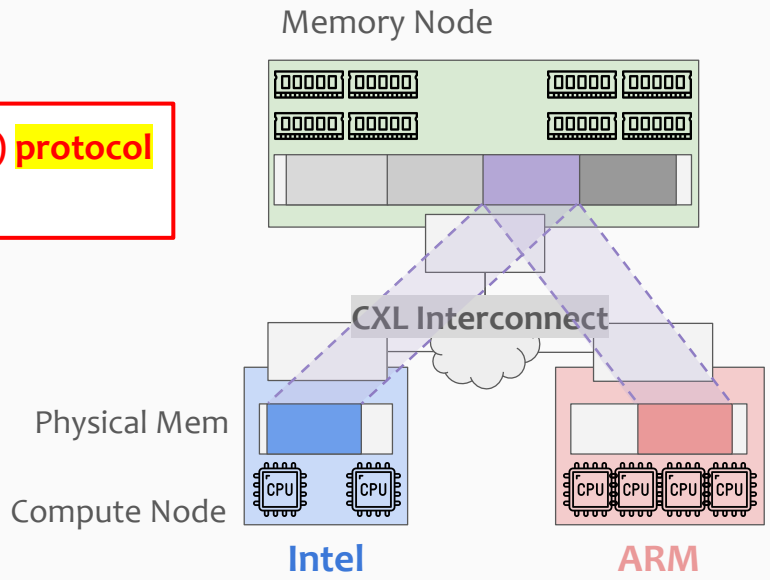
Cache coherence (CC) protocol mismatch



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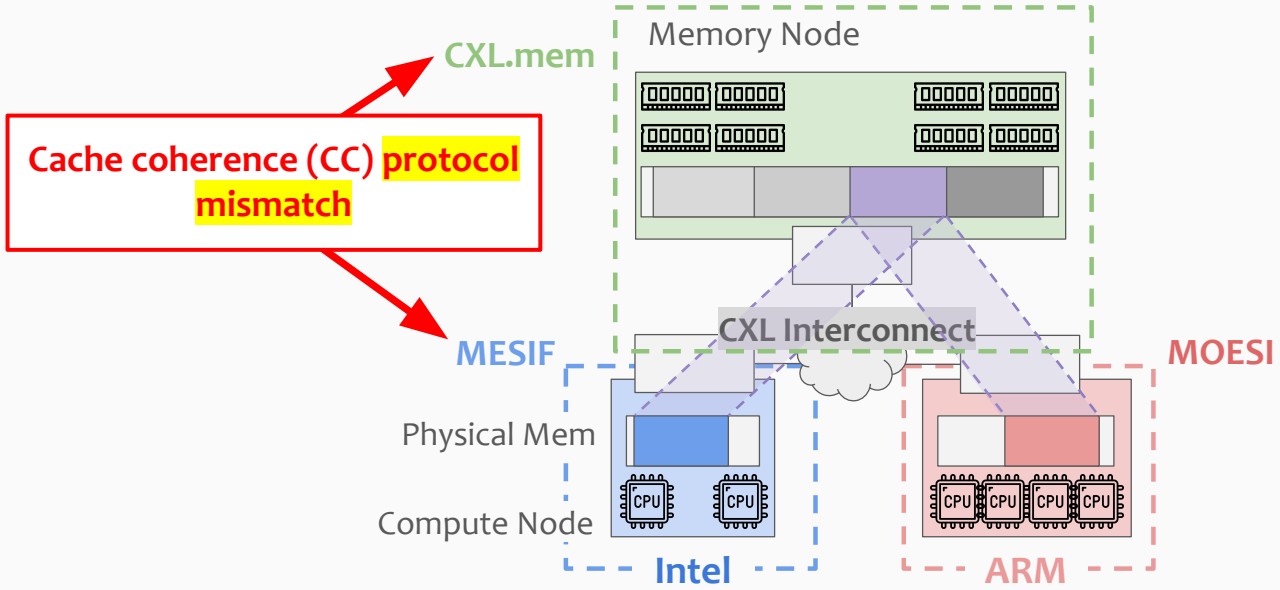

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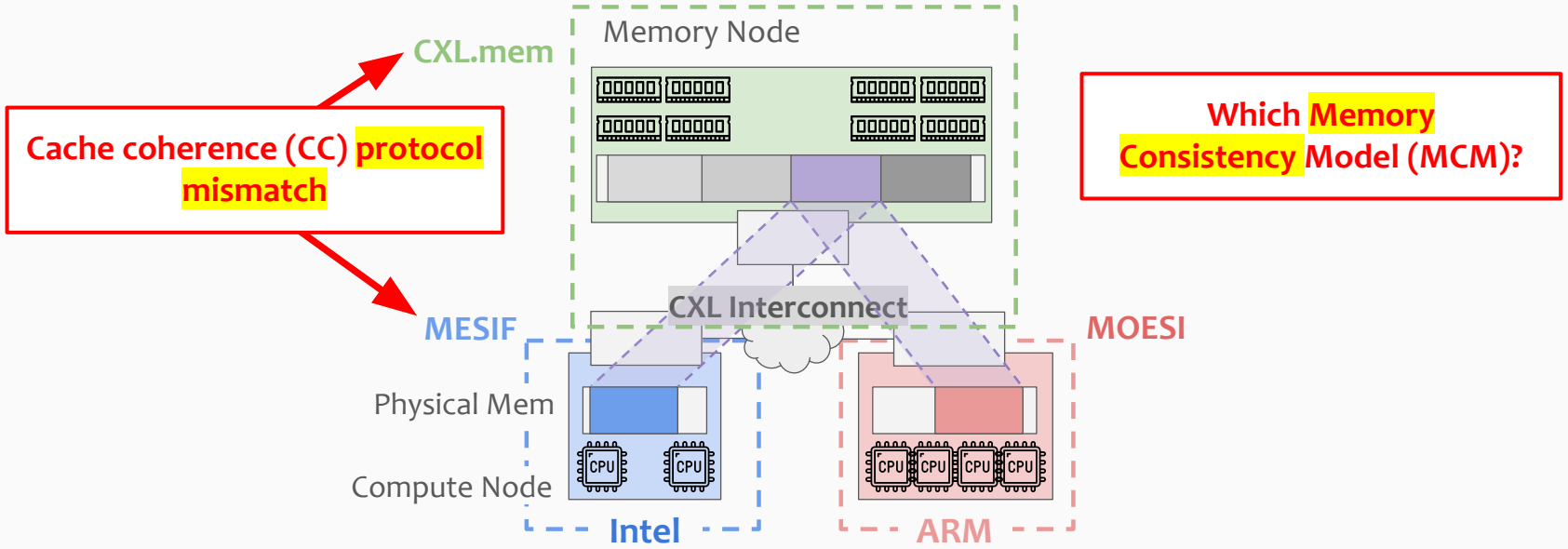

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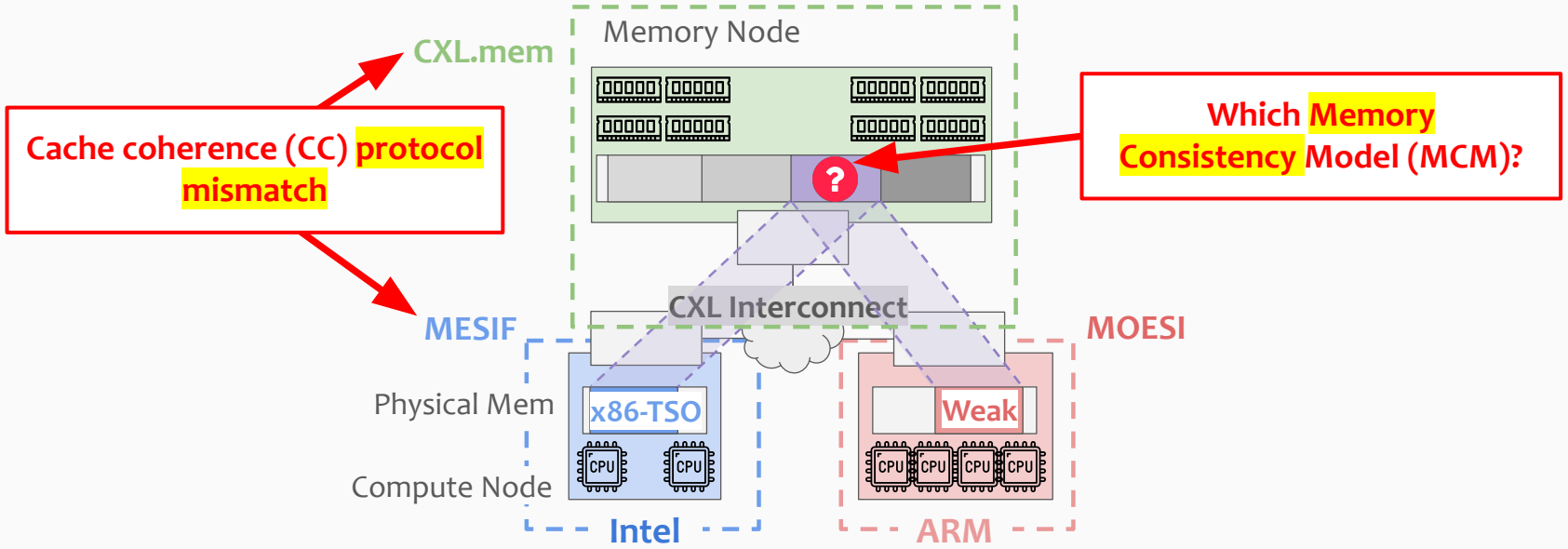

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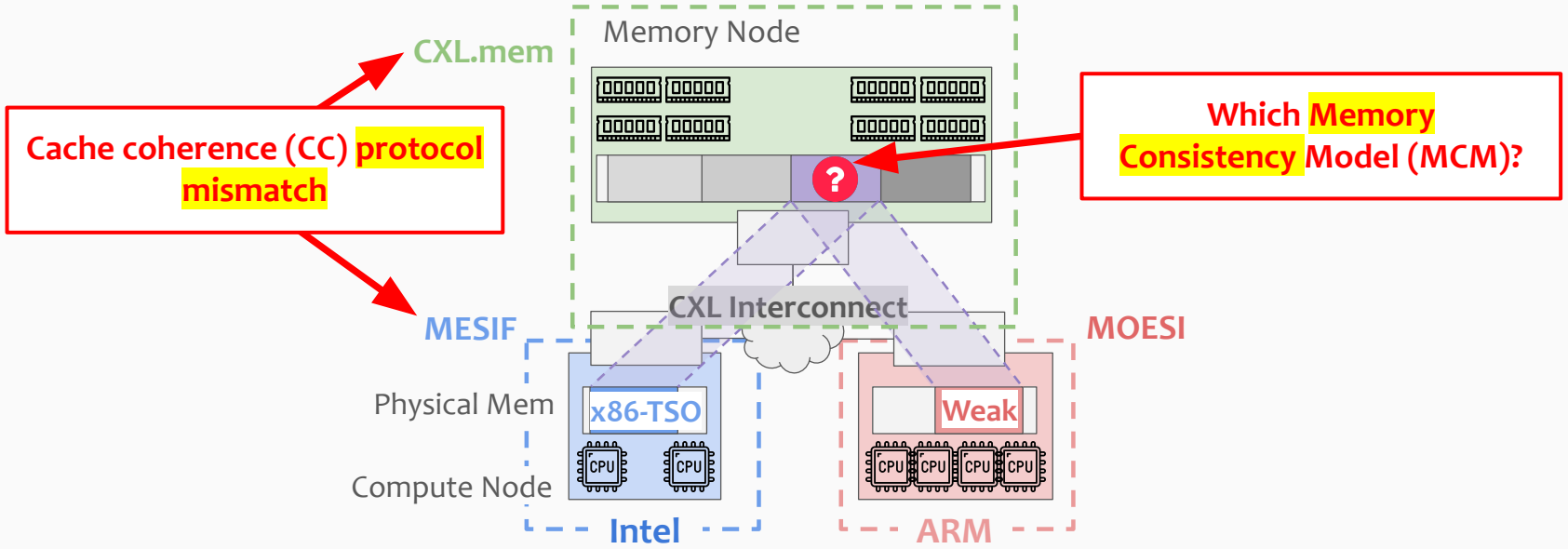
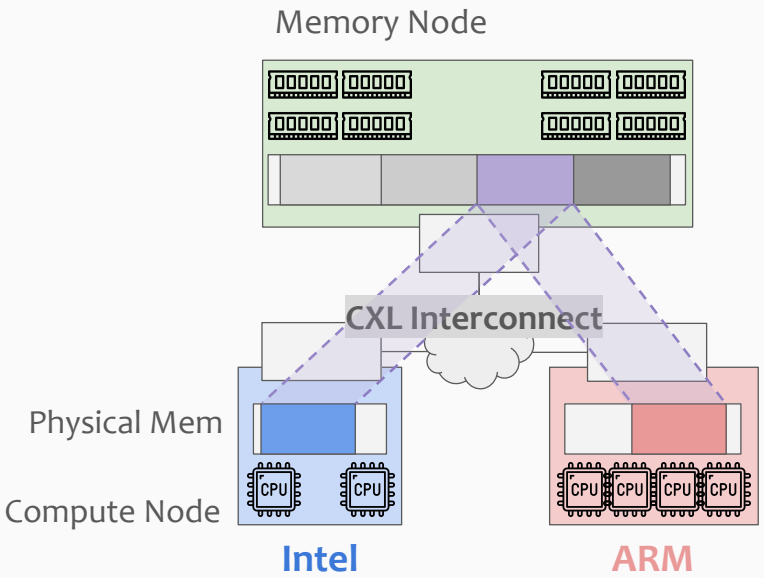


No, CXL does not support heterogeneous architectures

The answer: CXL Bridges[1]

To overcome the **semantic gap** created by **architecture heterogeneity** with **CXL**



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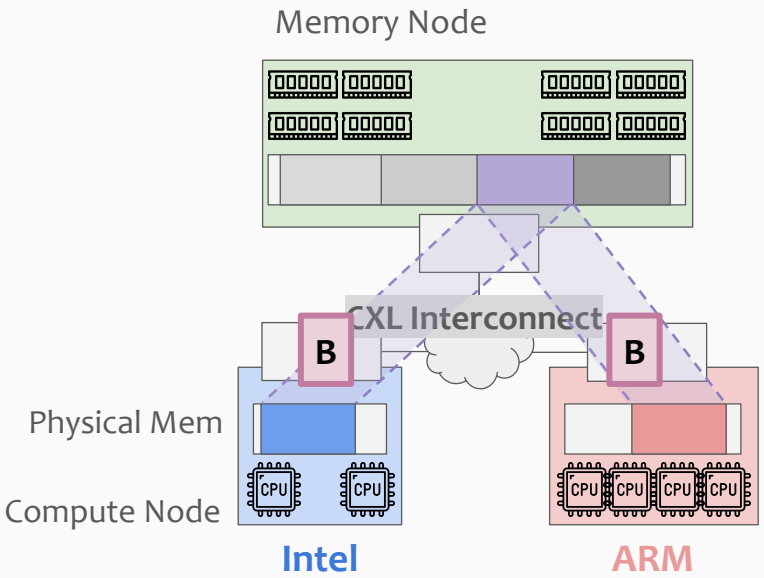

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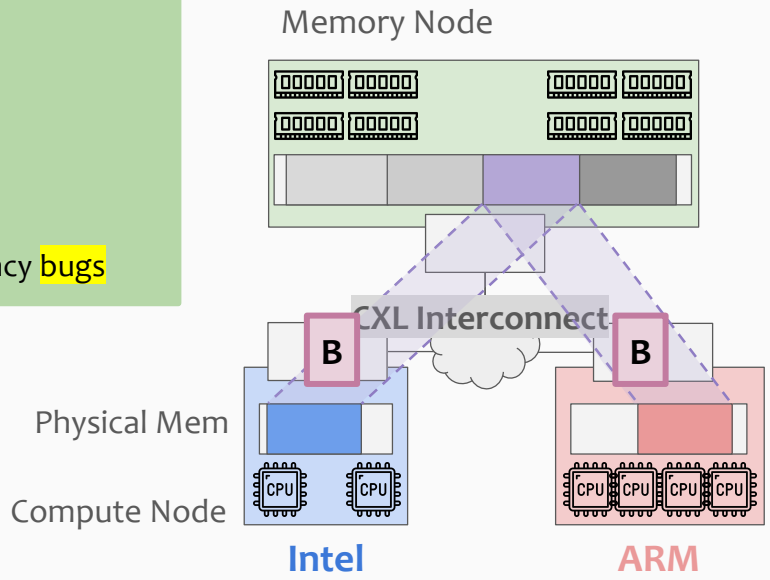
Intuition:

1. Translate *MESIF* / *MOESI* to ***"talk"*** with CXL.mem

2. Avoid memory consistency bugs



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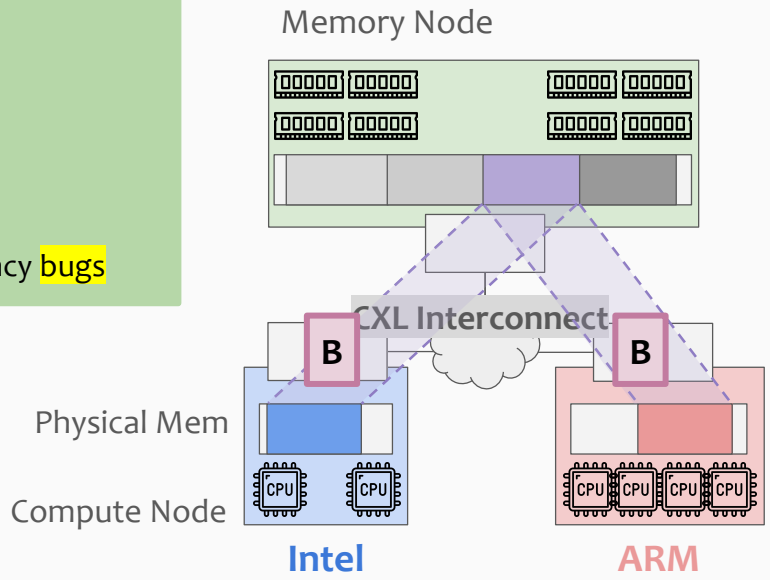

No guidance from **CXL specifications**

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Manual & ad-hoc

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Large state machines
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Problem Statement: How to systematically and correctly design CXL bridges for heterogeneous architectures?

Proposal: vCXLGen

Solution: Automatic synthesis of "*correct-by-construction*" CXL bridges from coherence protocol specifications for heterogeneous architectures

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Synthesize correct CXL **translations** from specifications

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Preserve **original MCMs** *by construction*

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Design Goals:

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3 Genericity

Applicable to any (**existing** and **upcoming**) architectures

Overview: **The vCXLGen** bridge generator

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Insight:

CXL Bridge: *compounding of finite state machines from* Host & CXL protocols

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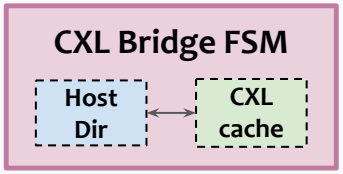

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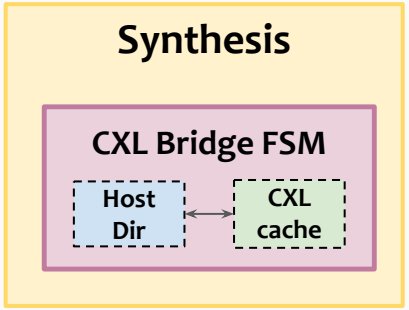

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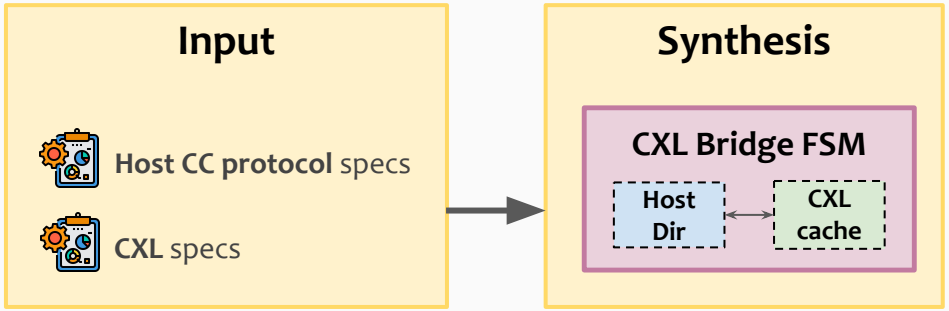

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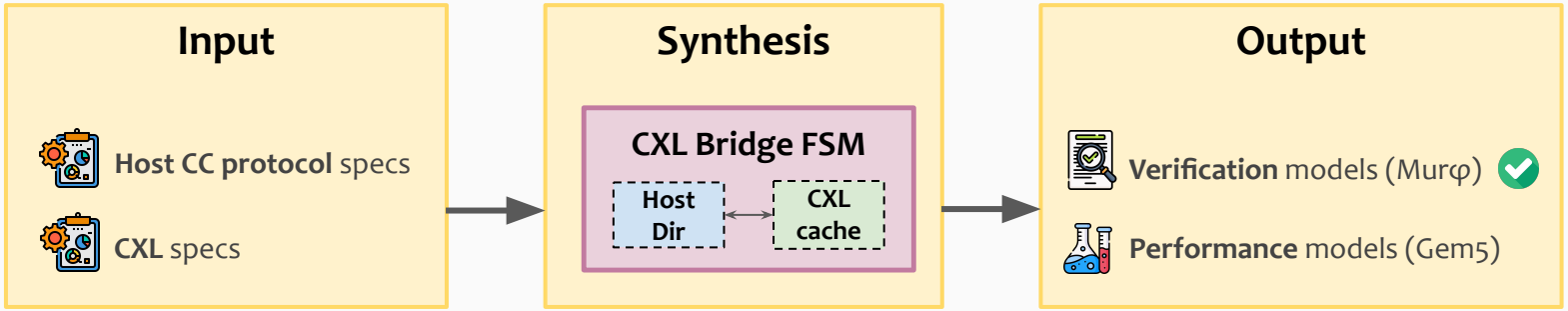

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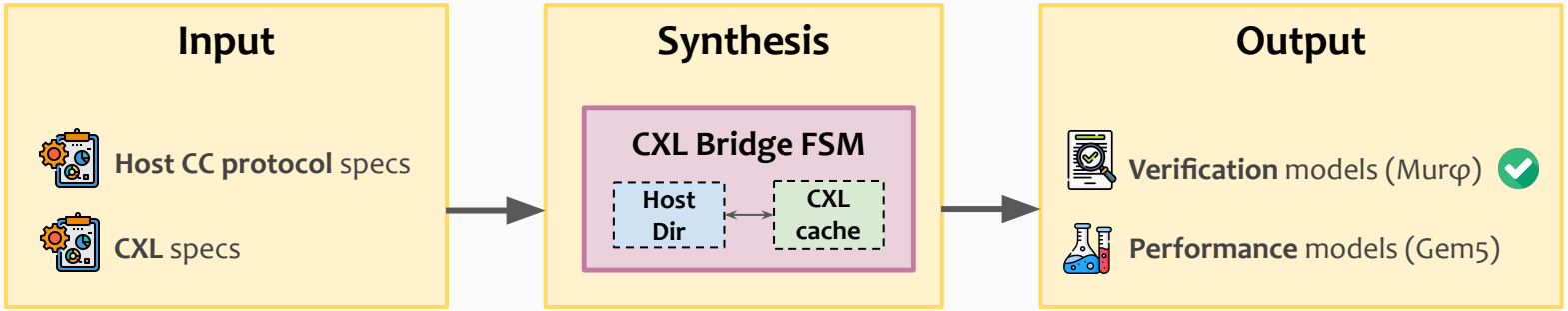

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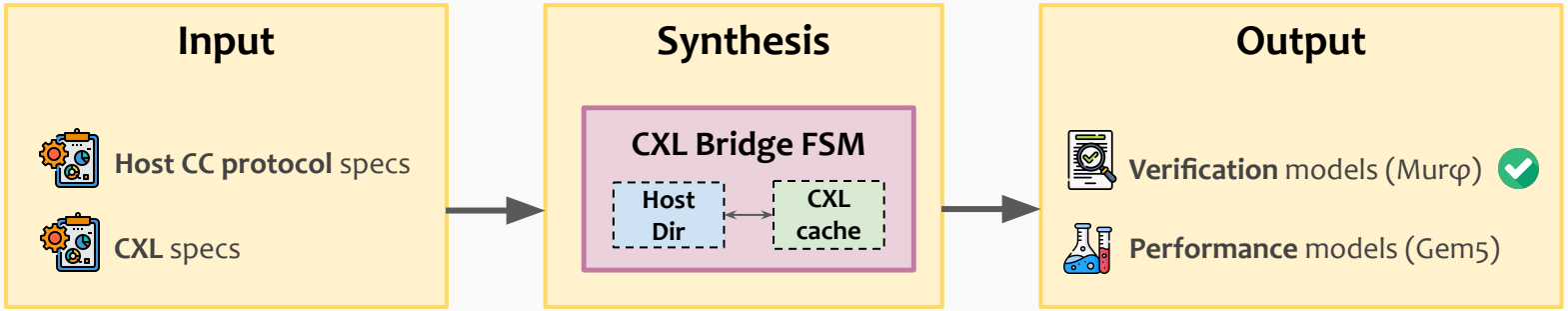

Contributions:

Generic synthesis algorithm
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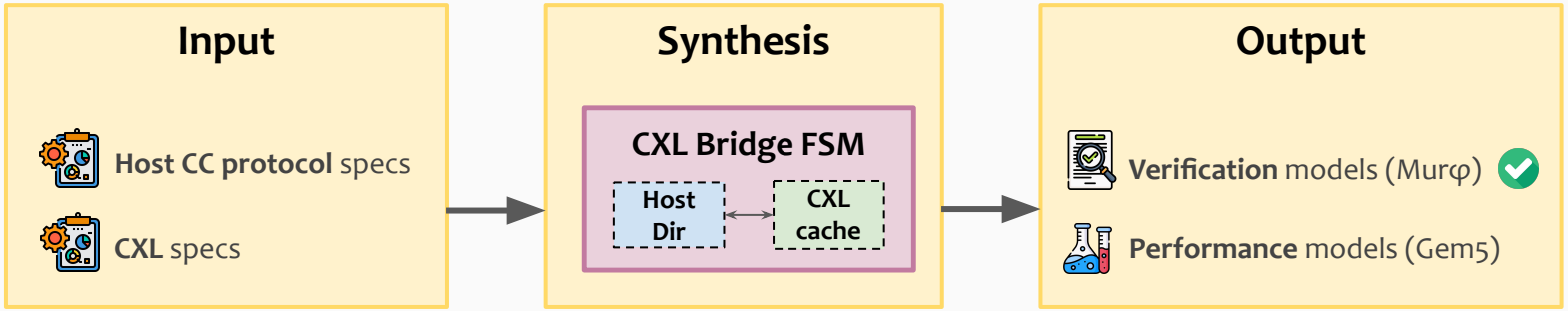
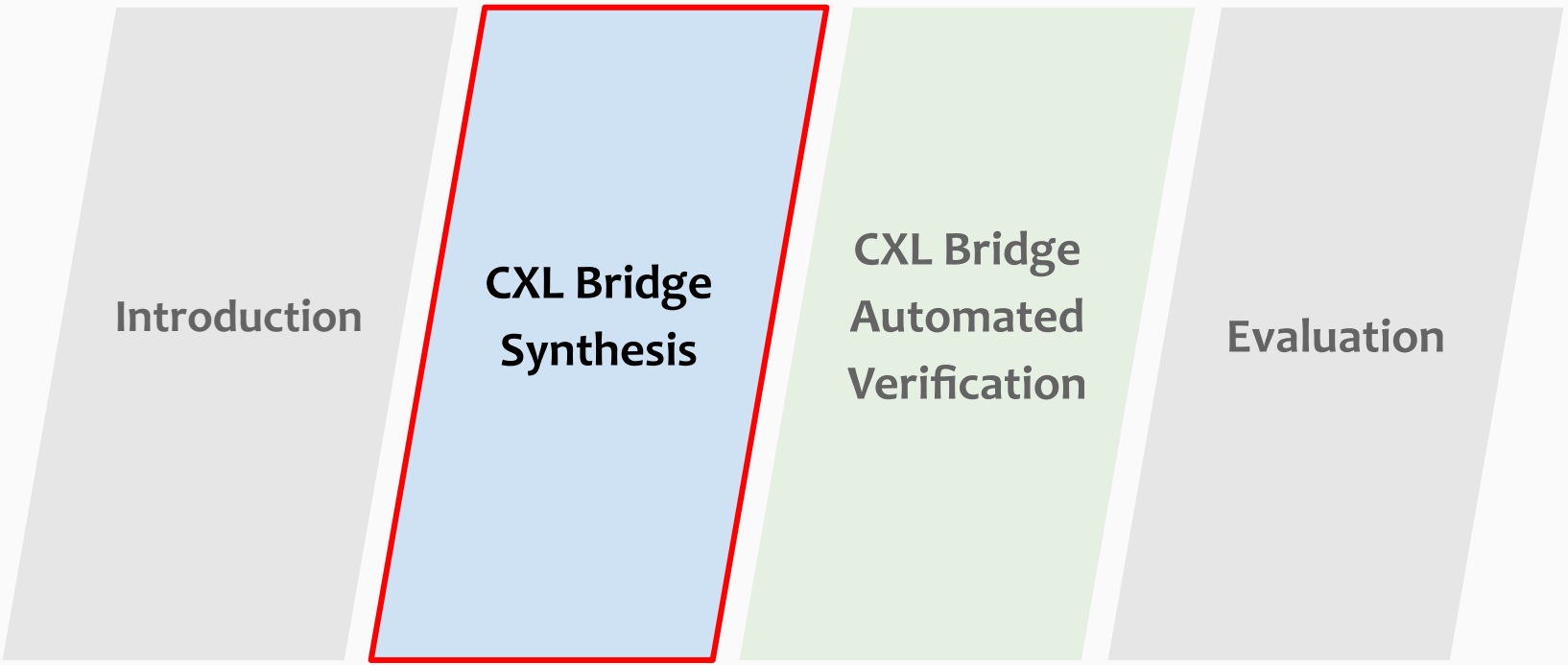


Contributions:

Generic synthesis algorithm for CXL bridges

Automated correctness verification for CXL bridges

Outline


Introduction
CXL Bridge Synthesis
CXL Bridge Automated Verification
Evaluation

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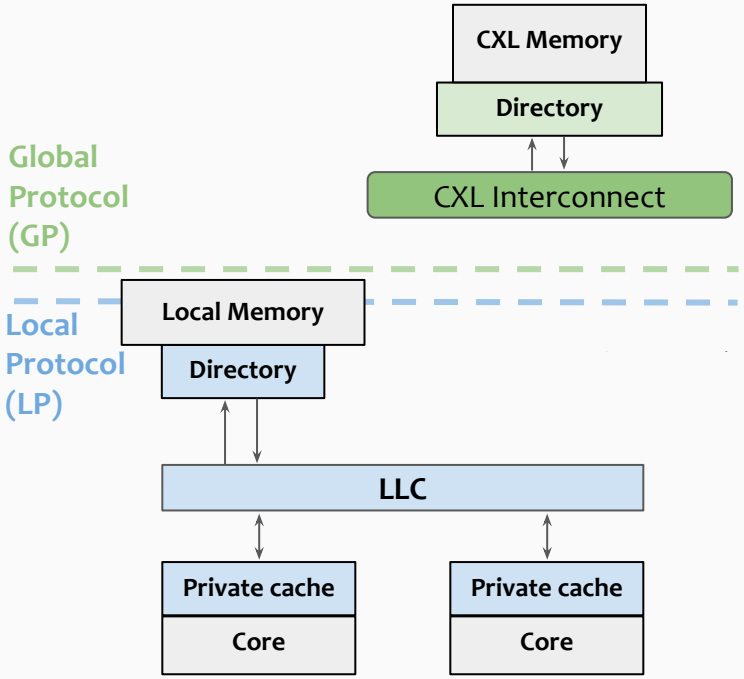

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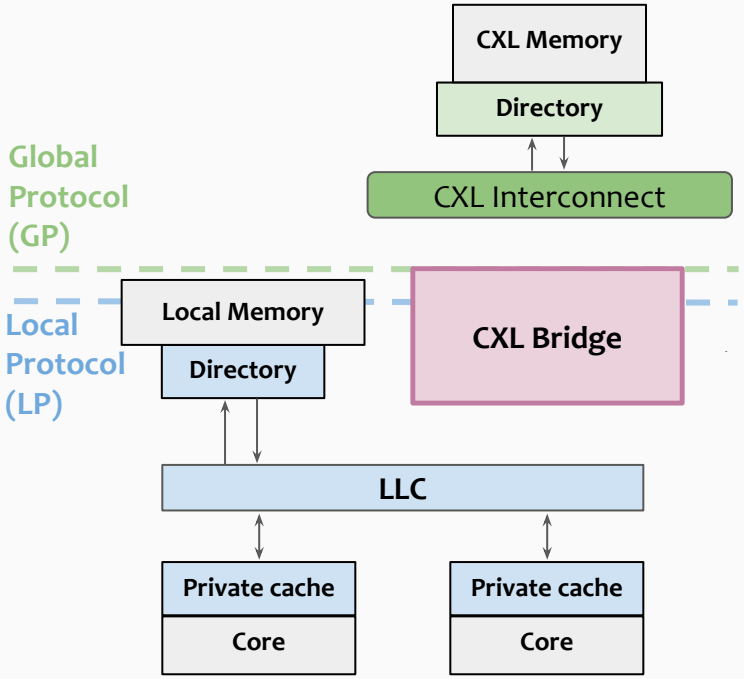

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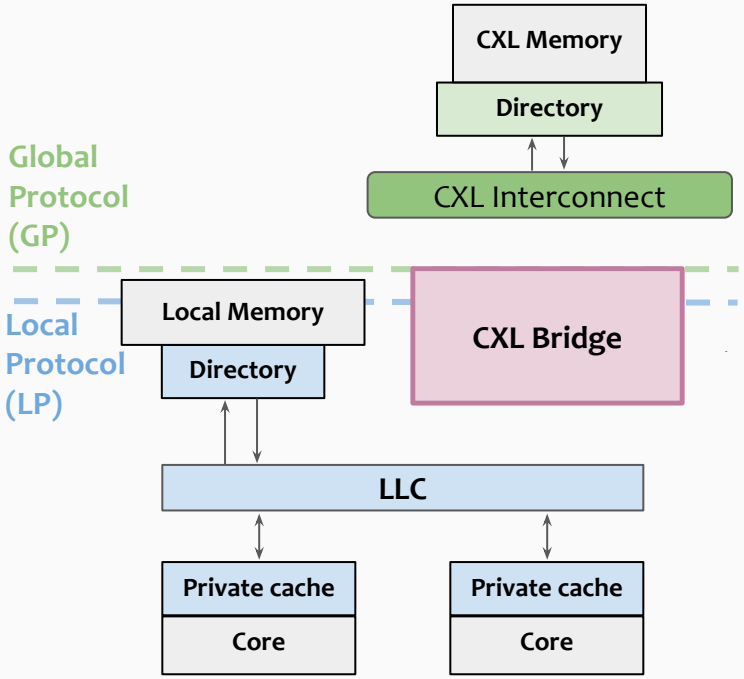

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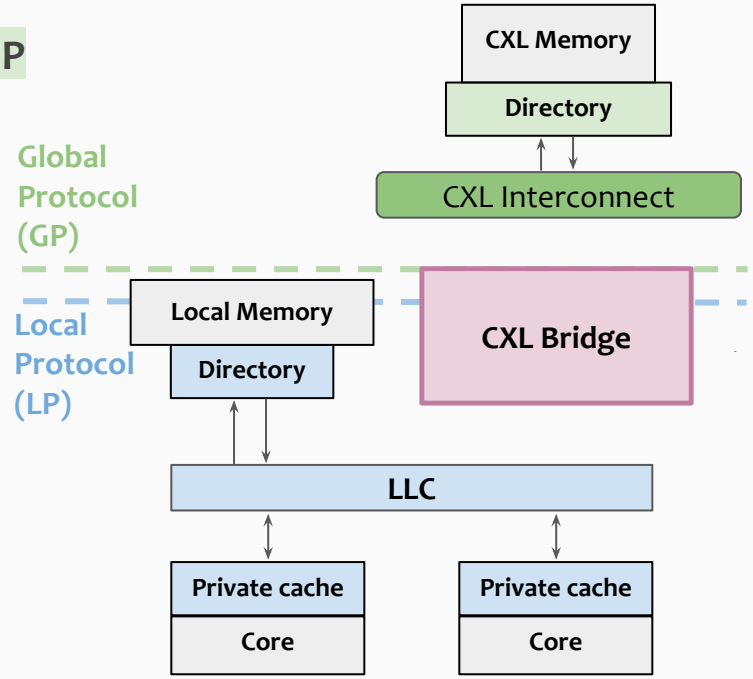

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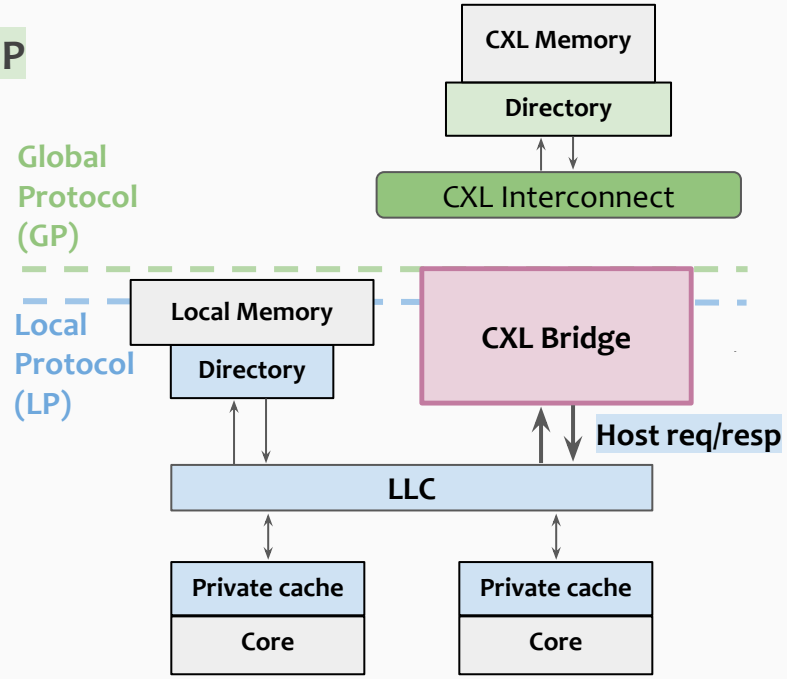

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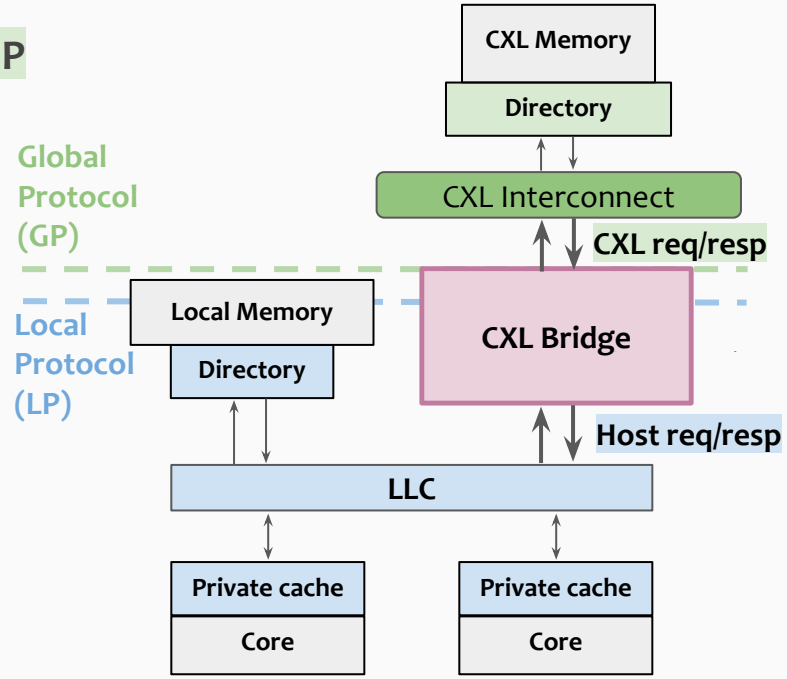

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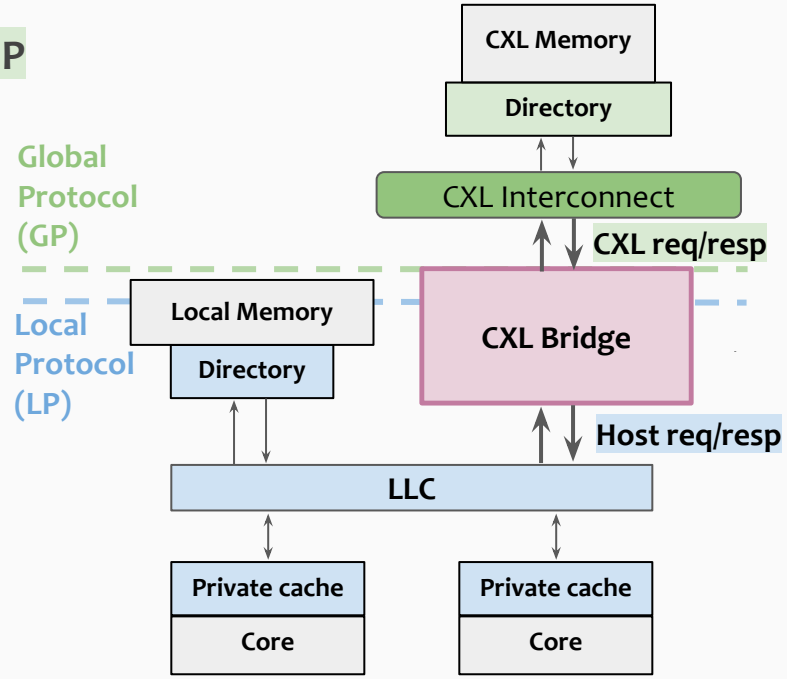

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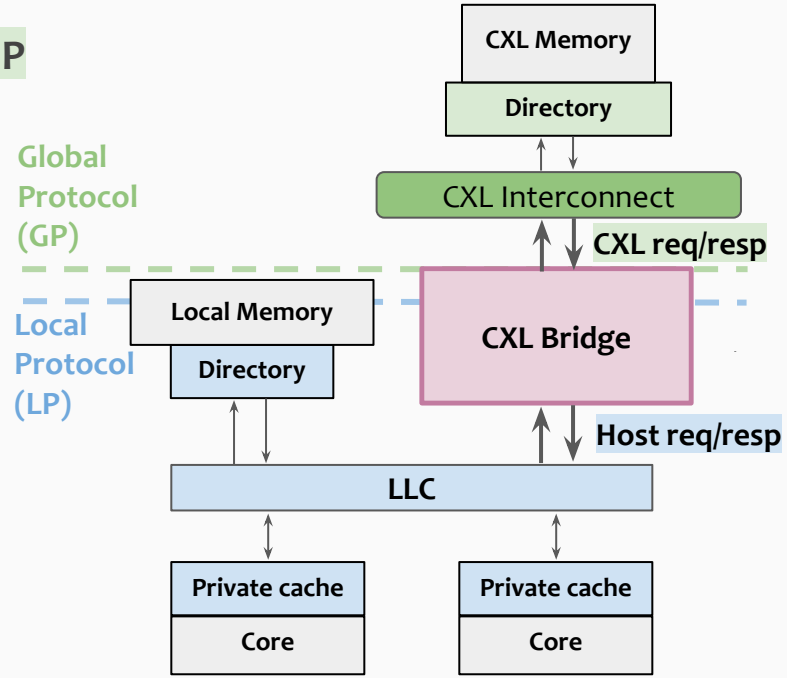

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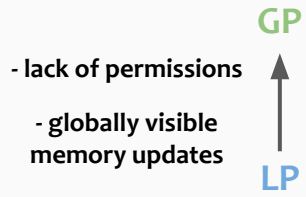

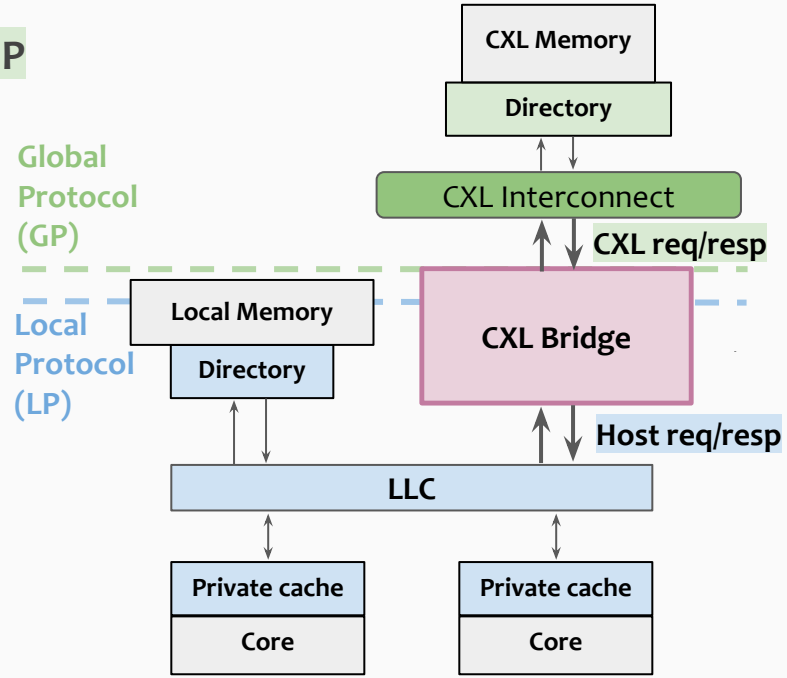

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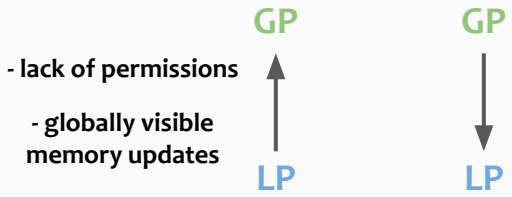

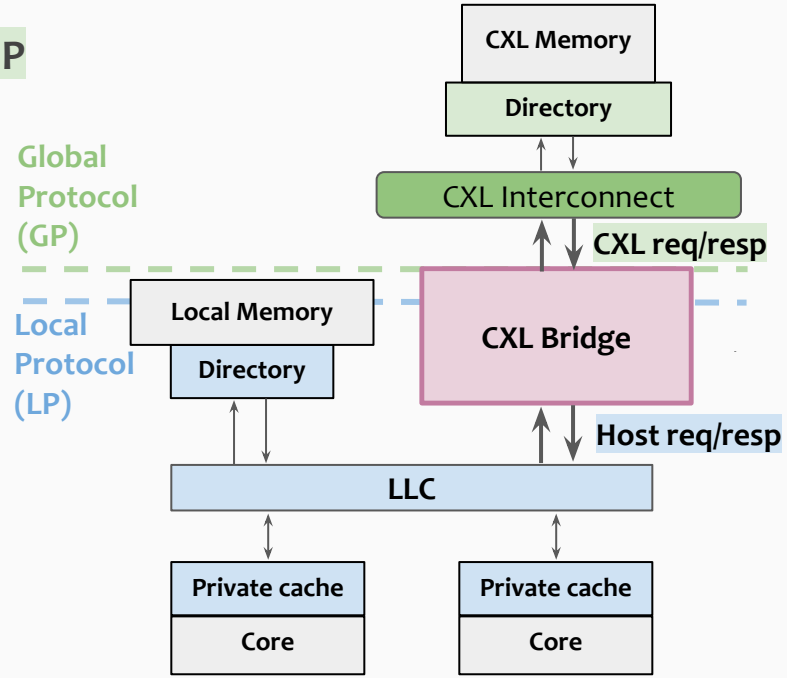

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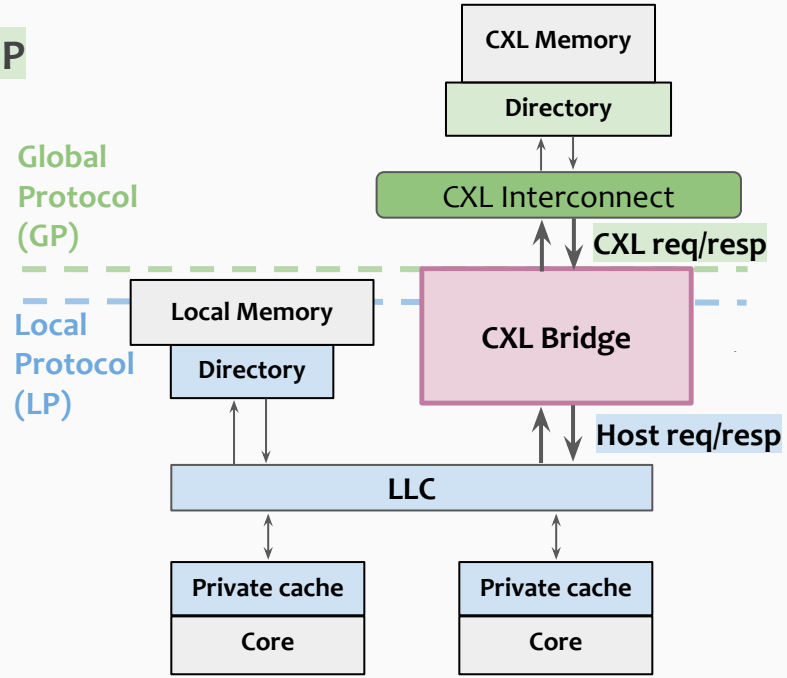

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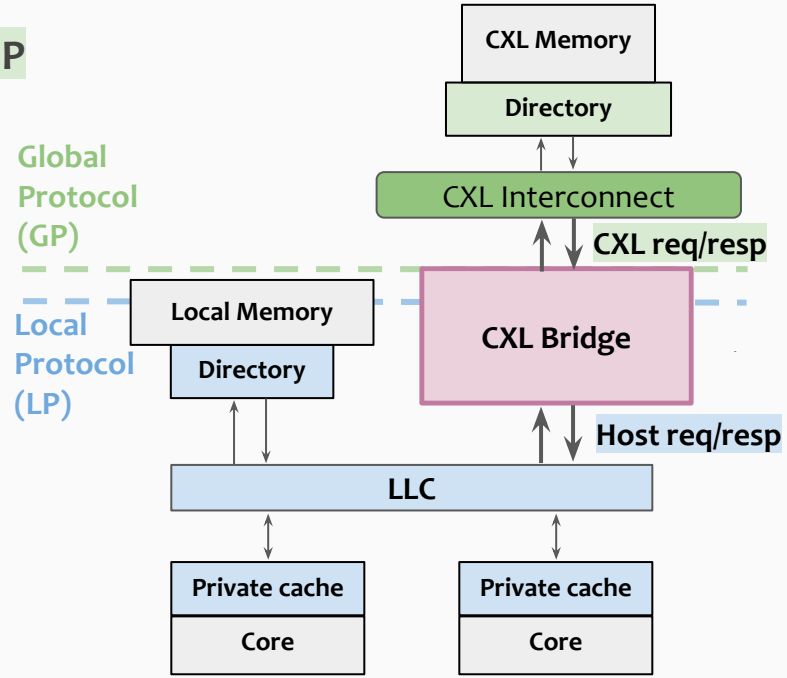

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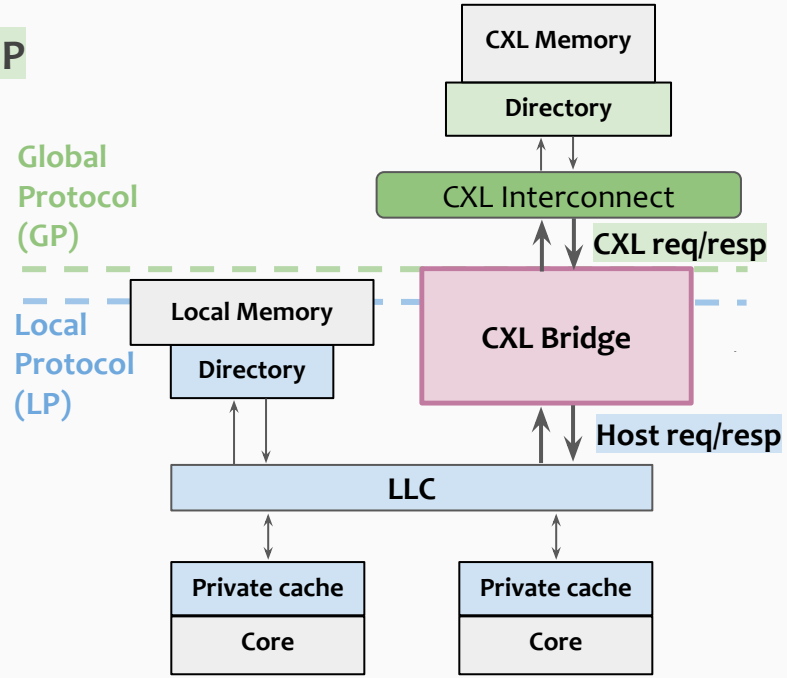

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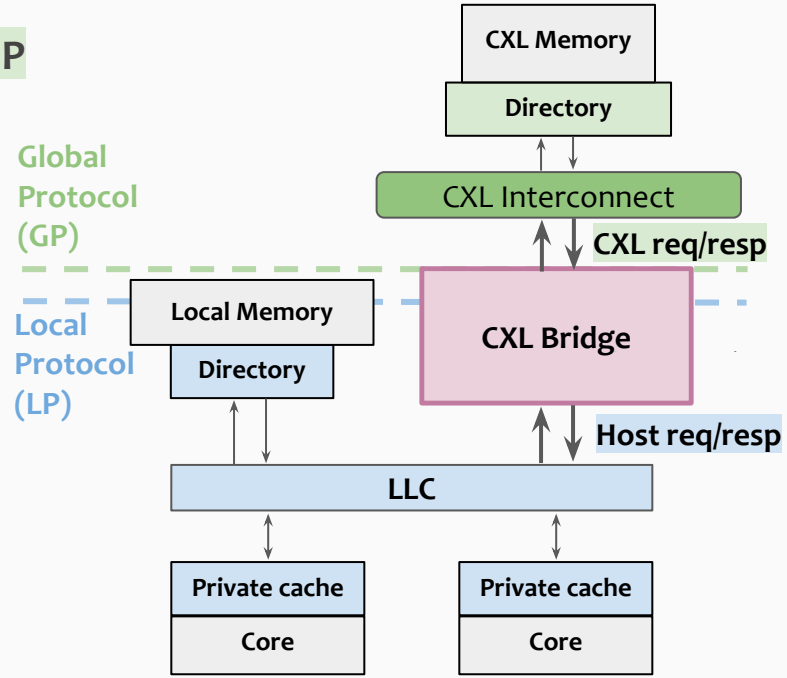
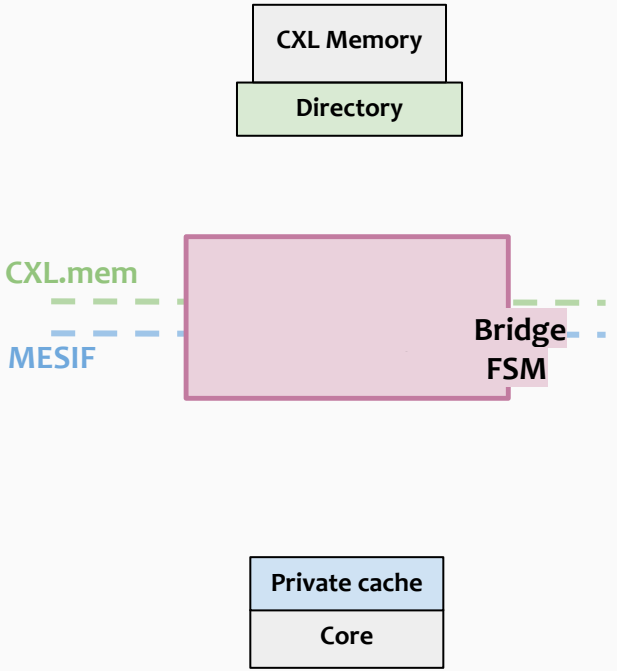
b. *Semantically correct* request translations

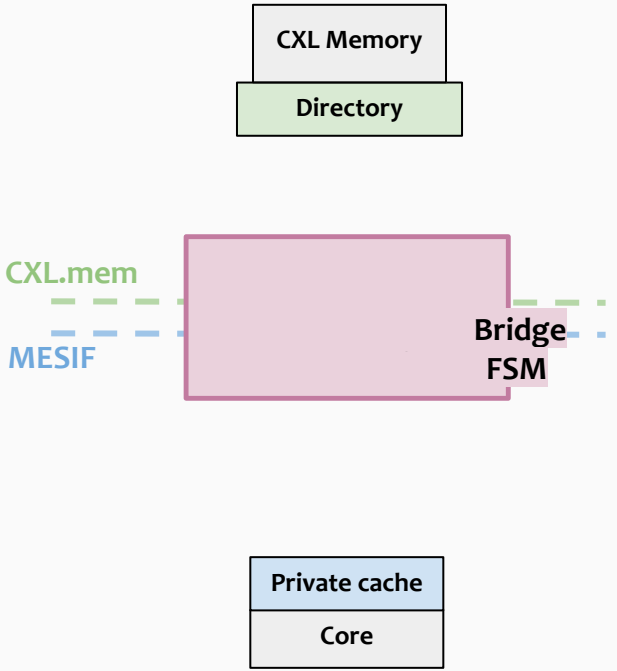


Synthesis: **Semantic translation**



Synthesis: **Semantic translation**

How to generate the bridge FSM?



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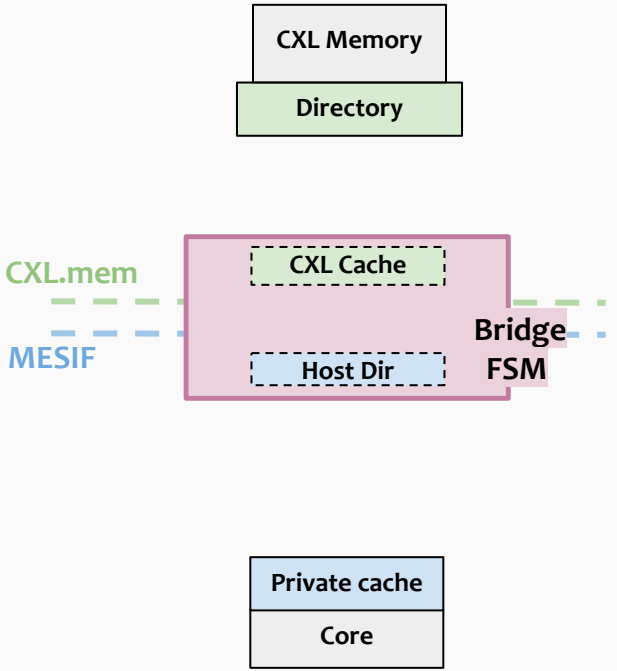

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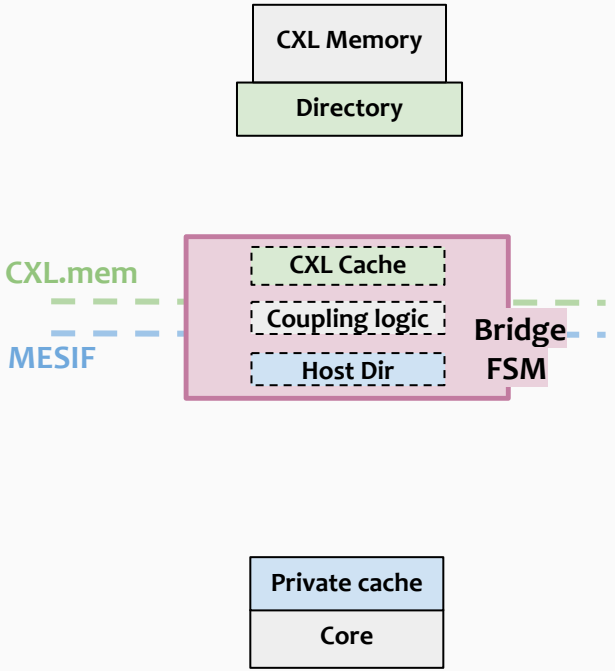
How to generate the bridge FSM?



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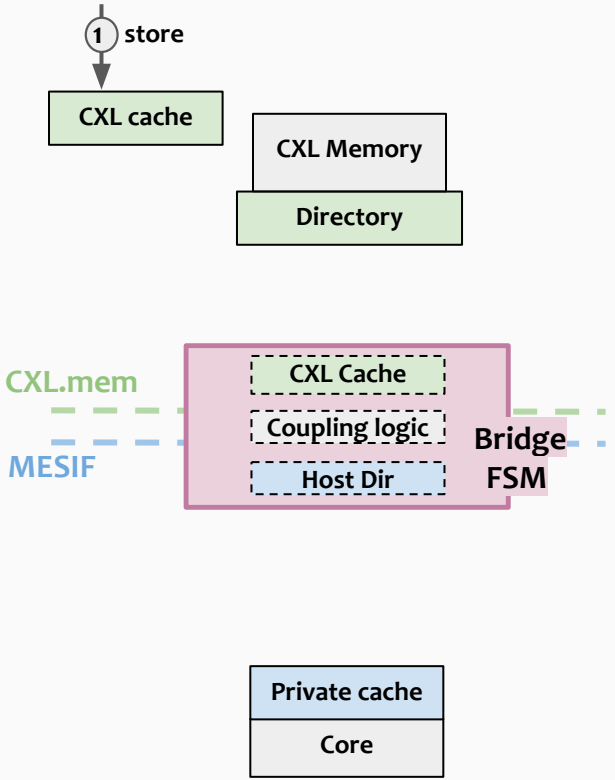
How to generate the bridge FSM?



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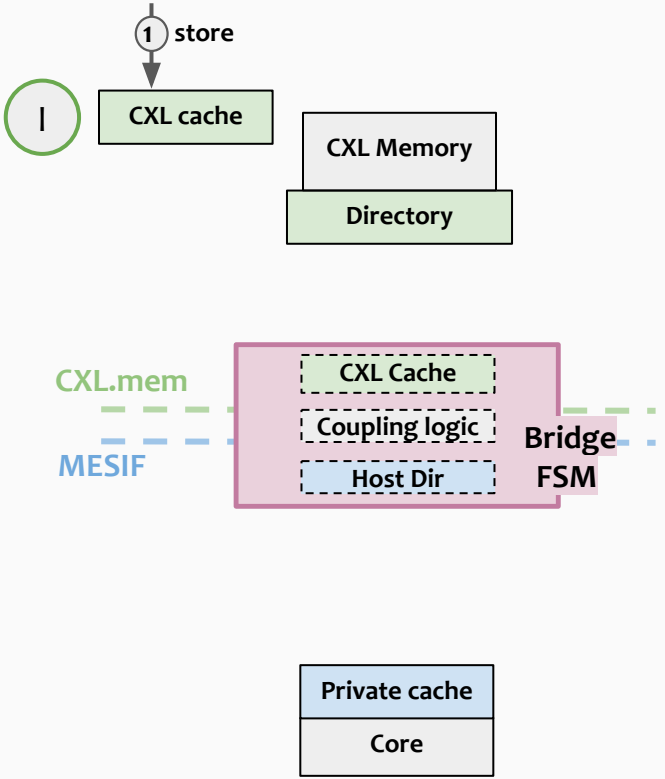
How to generate the bridge FSM?



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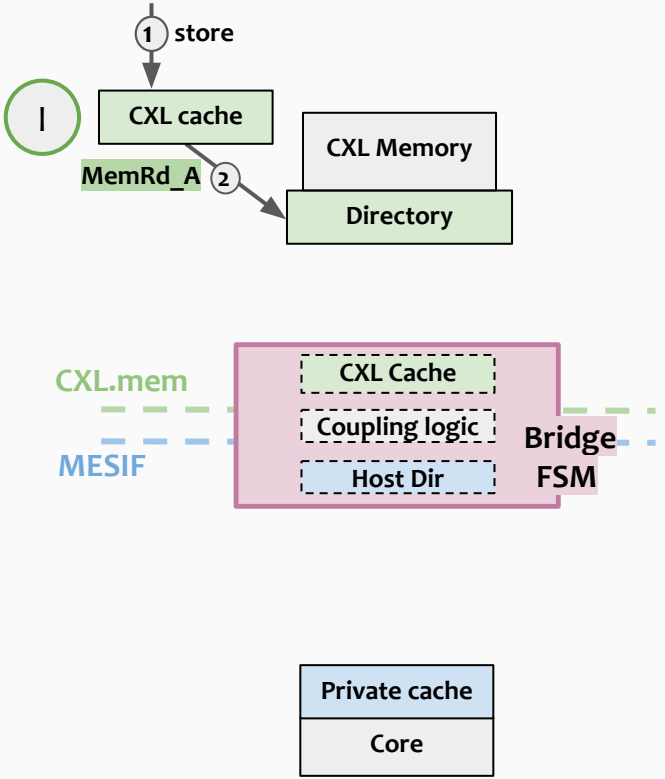

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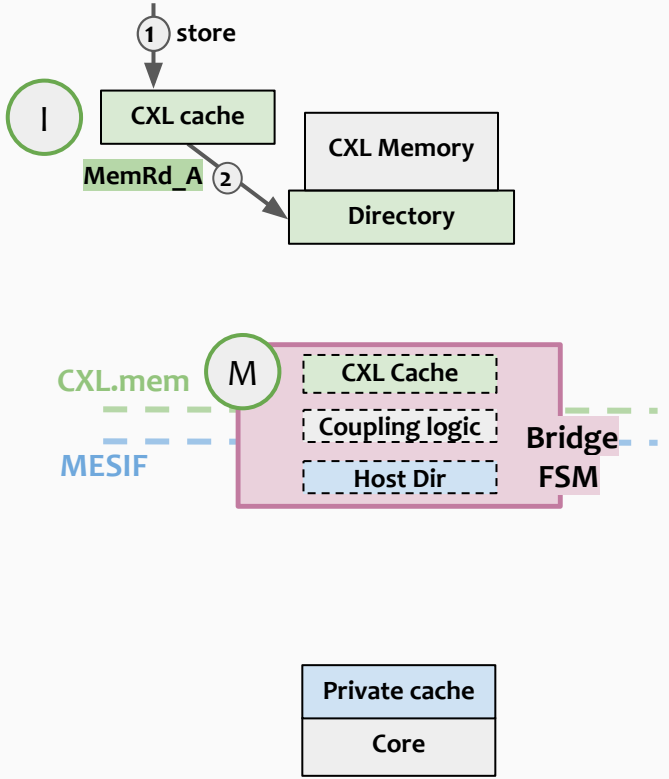
How to generate the bridge FSM?



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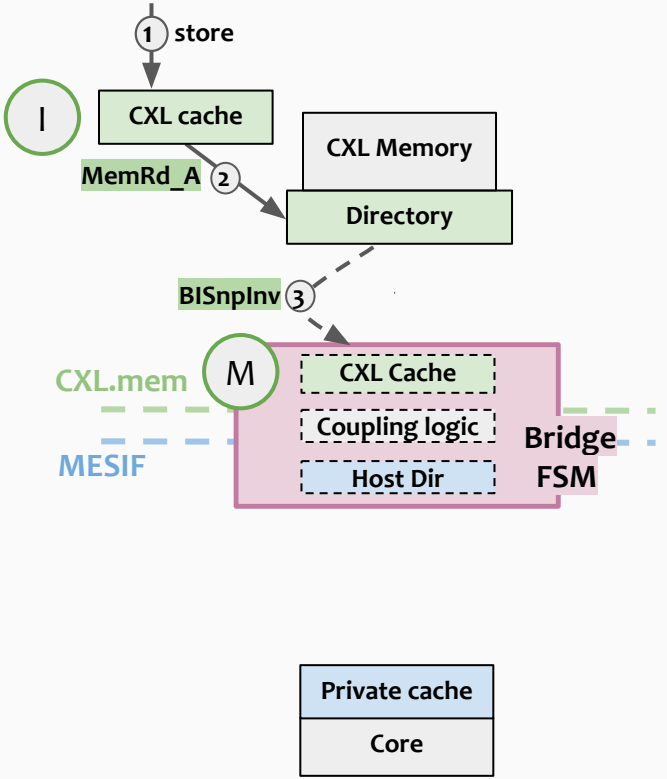

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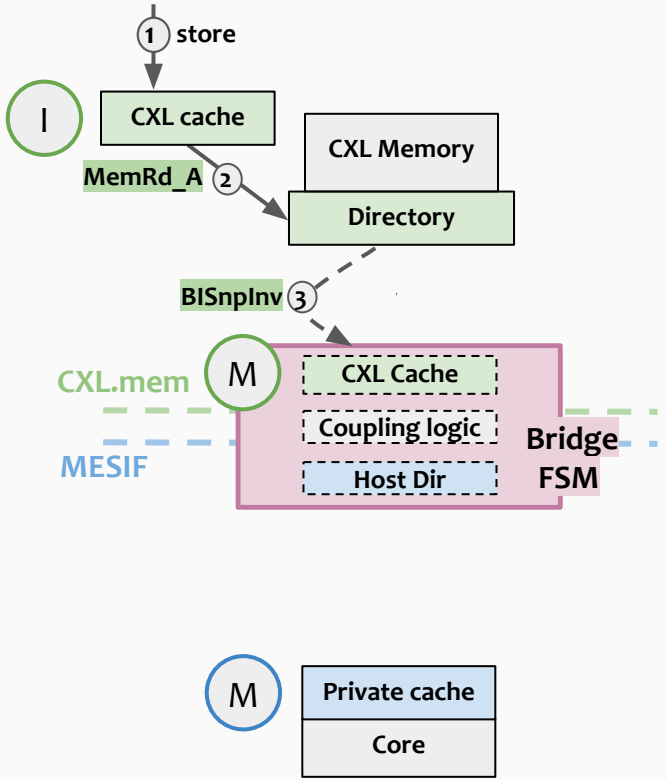

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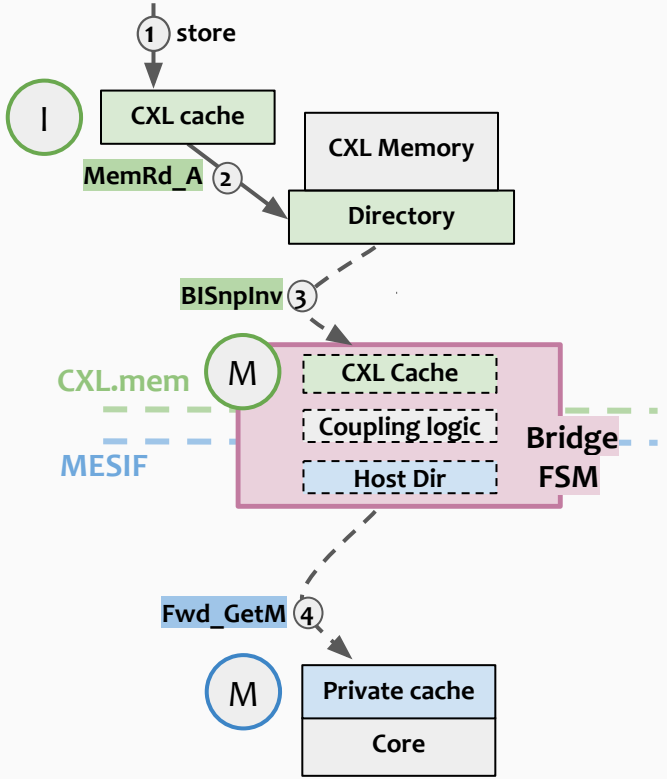

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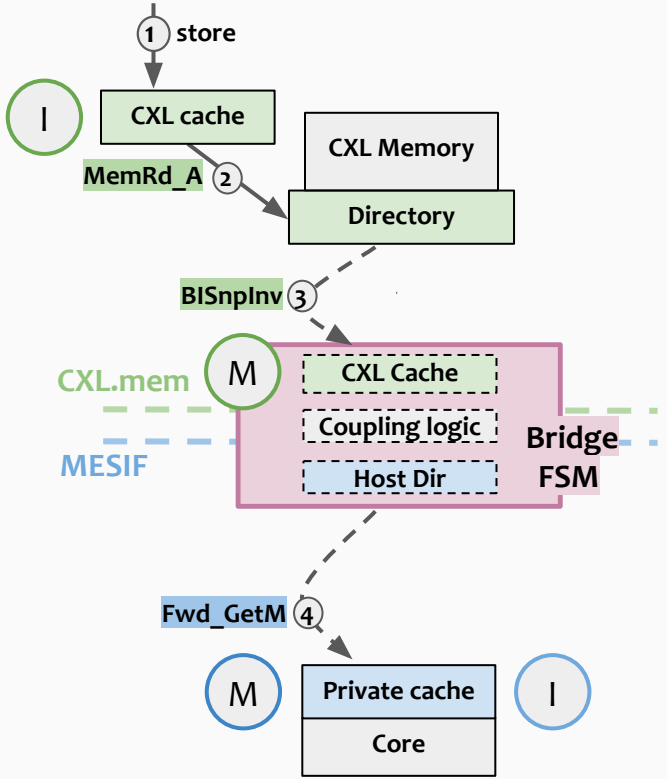

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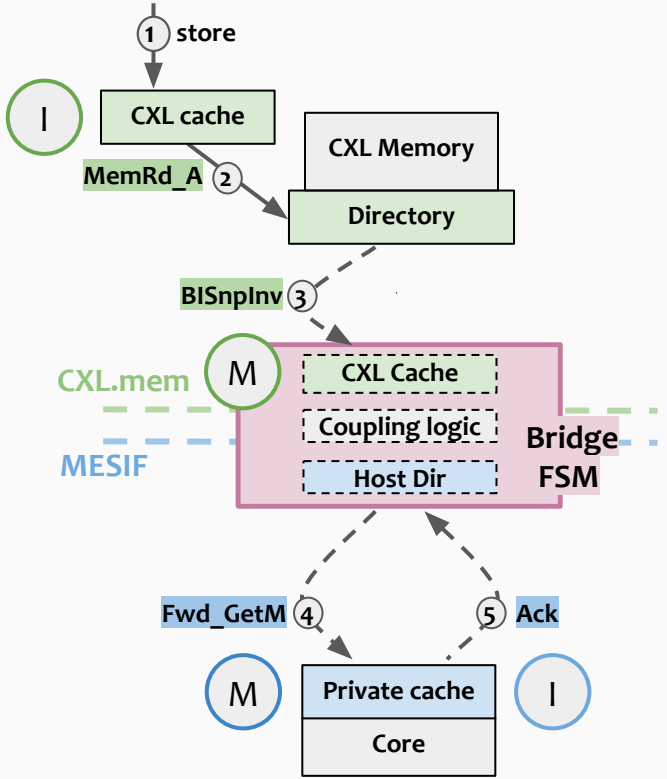

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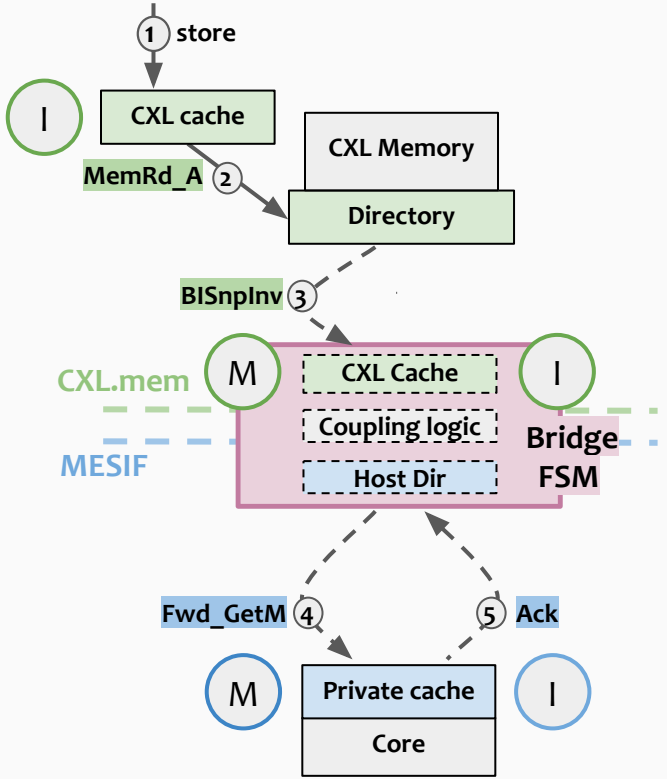

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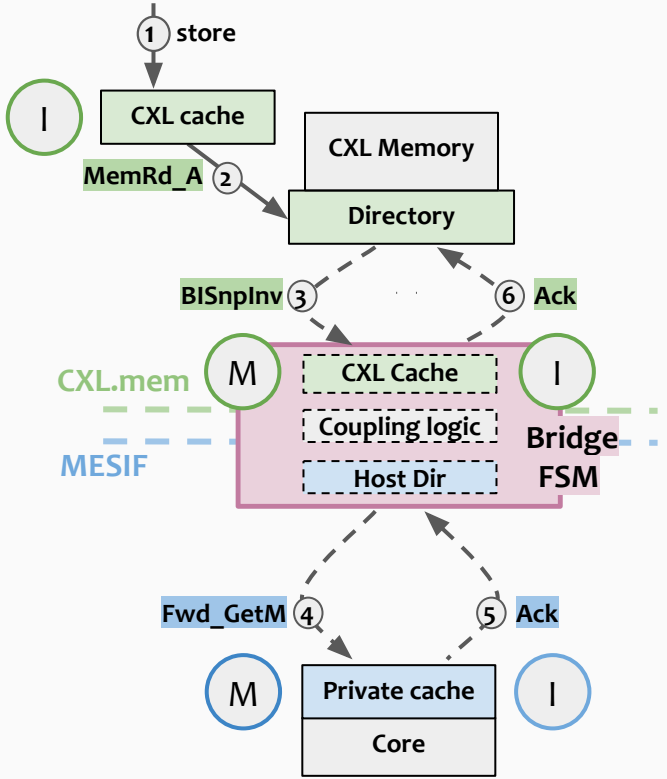

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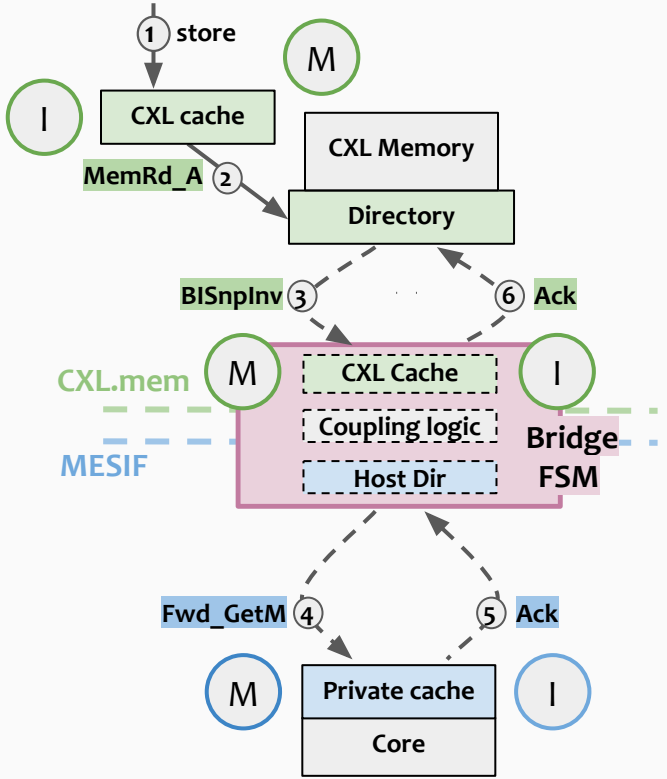
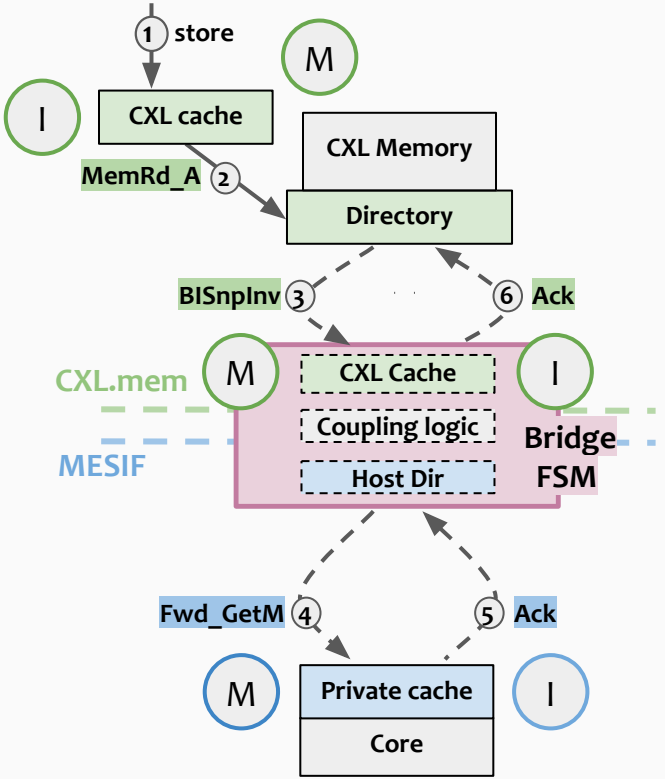


Synthesis: **Semantic translation**

How to generate the bridge FSM?

Static analysis of Host Dir & CXL Cache FSMs**:**



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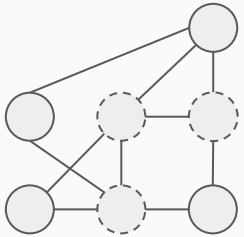
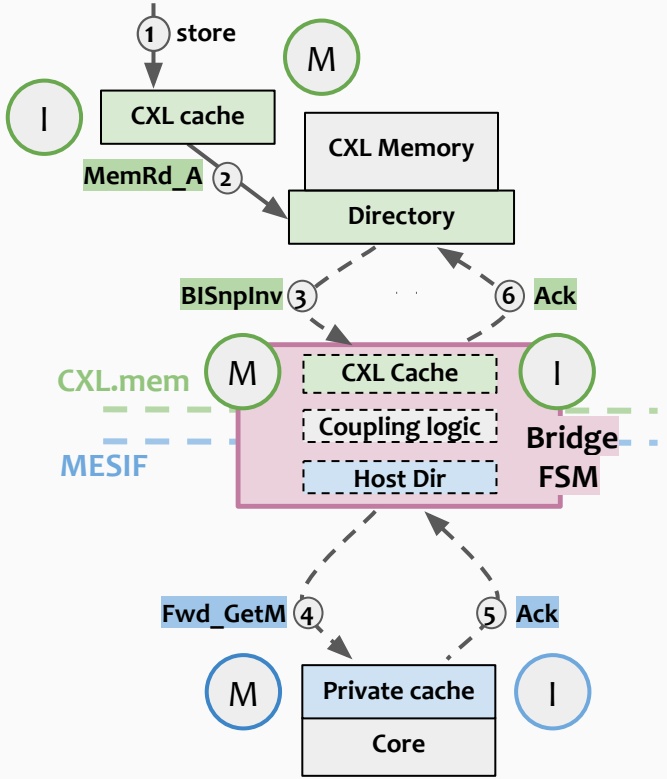
Static analysis of Host Dir & CXL Cache FSMs**:**

Host Dir





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Static analysis of Host Dir & CXL Cache FSMs:

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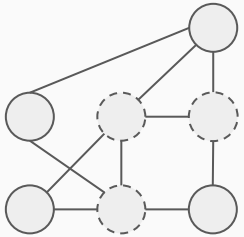
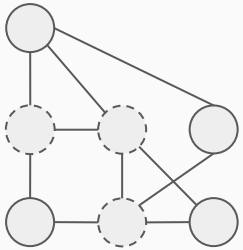
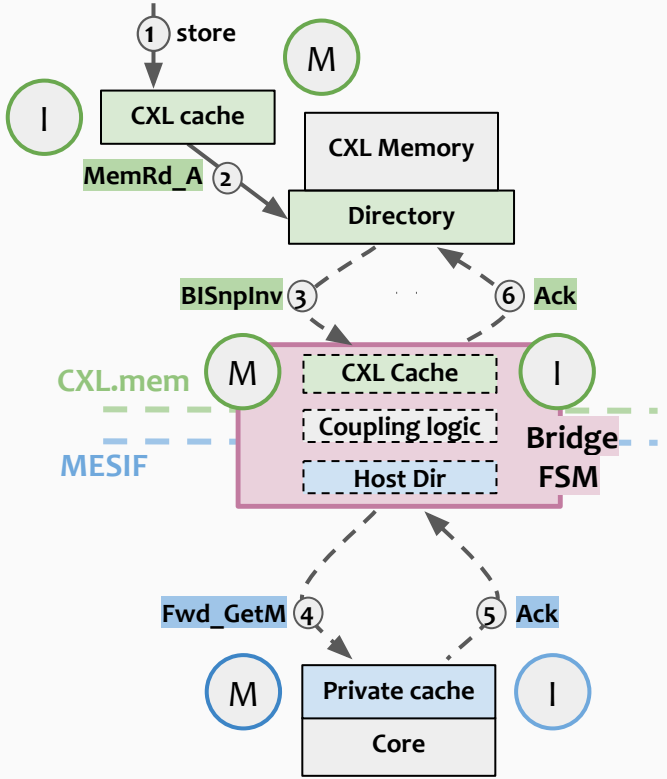


CXL Cache



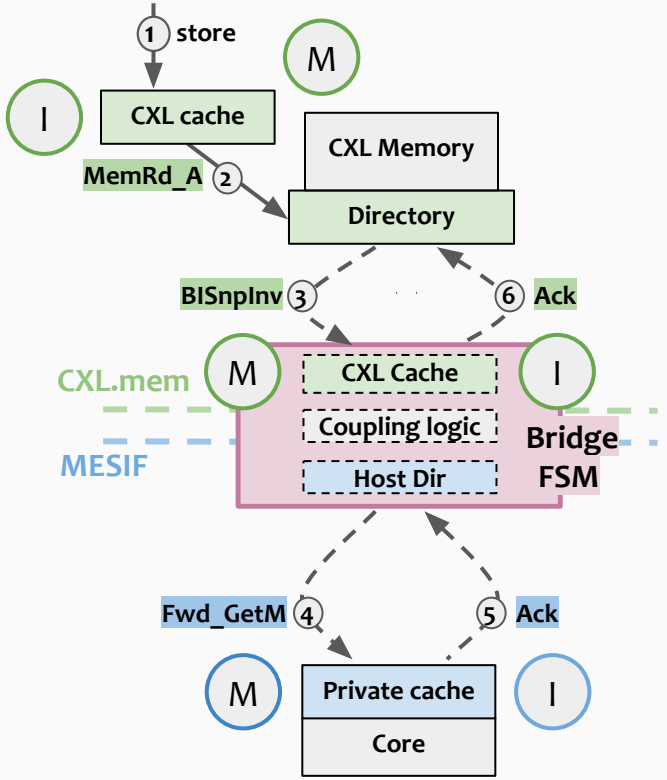


Synthesis: **Semantic translation**

How to generate the bridge FSM?

Static analysis of Host Dir & CXL Cache FSMs:

Host Dir Coupling logic CXL Cache



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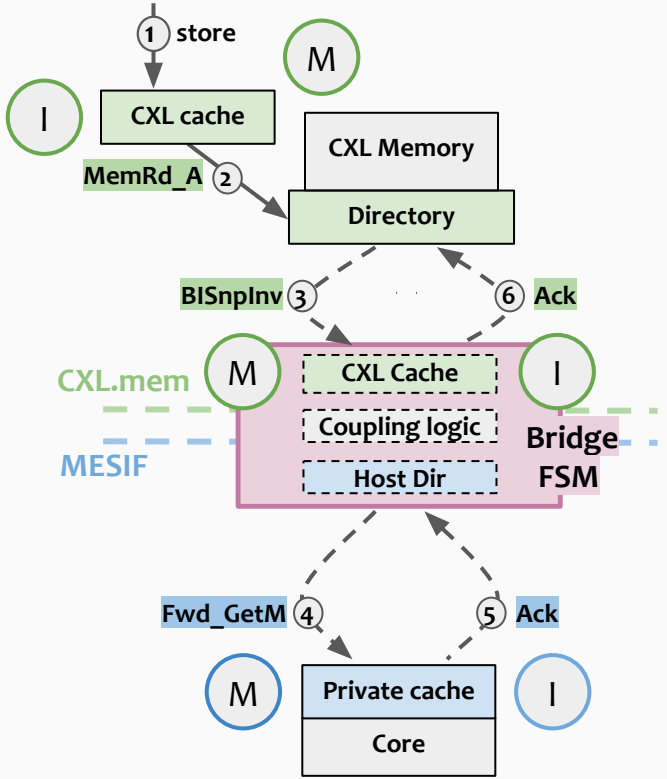

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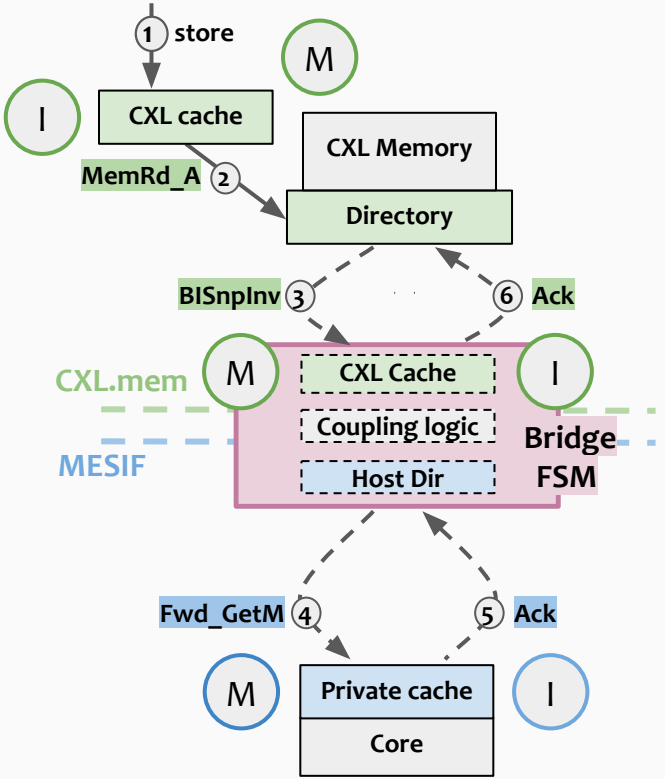

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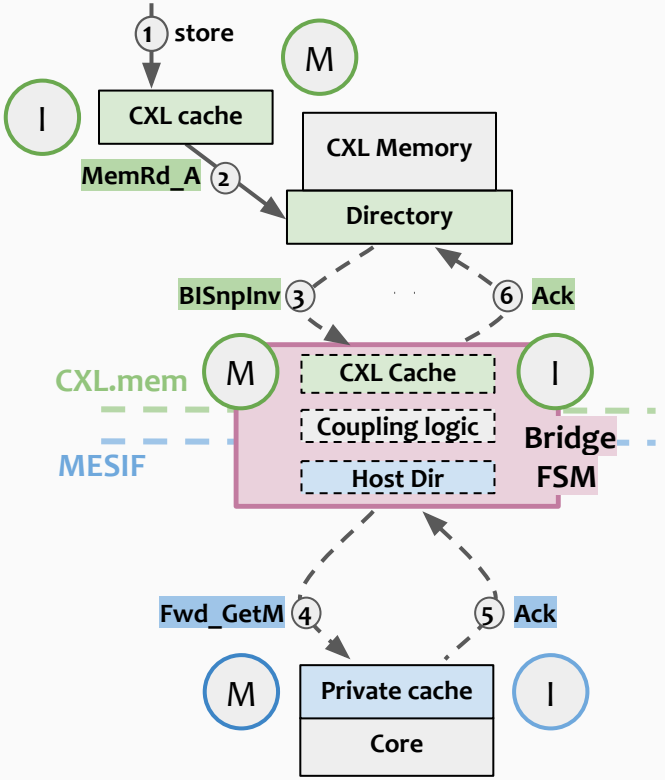


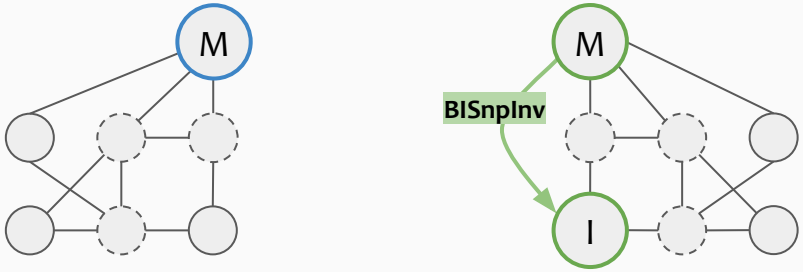
1. *Identify requests that must propagate*

Synthesis: **Semantic translation**

How to generate the bridge FSM?

Static analysis of Host Dir & CXL Cache FSMs:

Host Dir | Coupling logic | CXL Cache



(cache permission downgrade)

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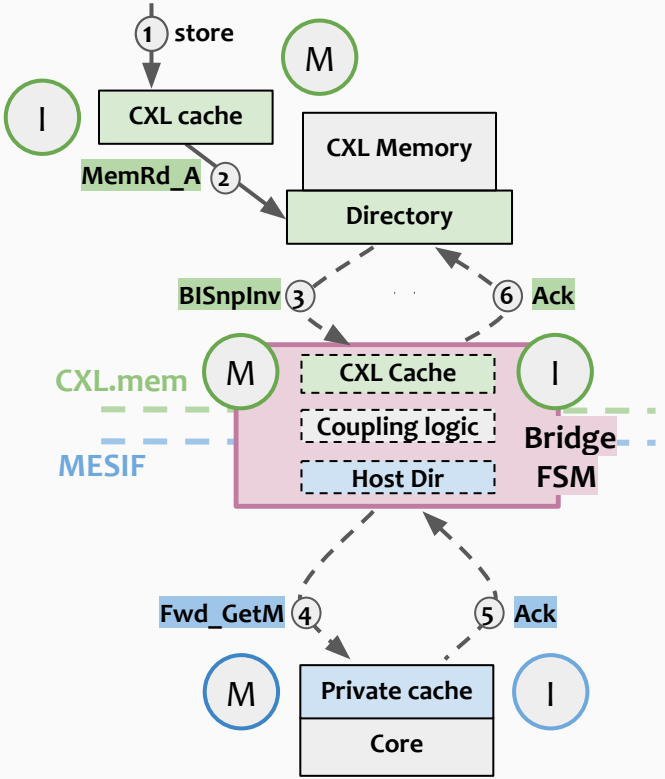

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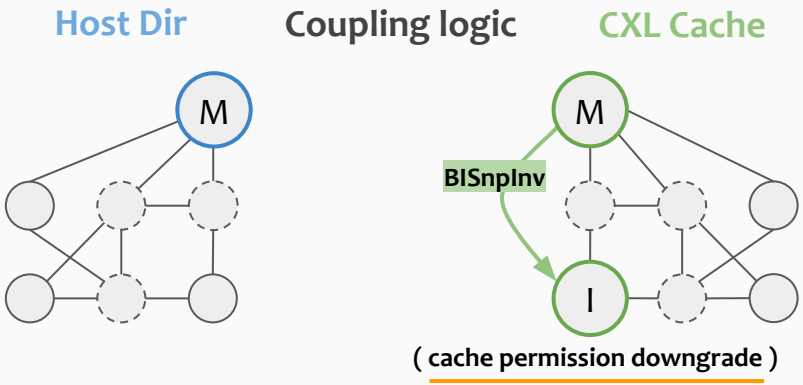

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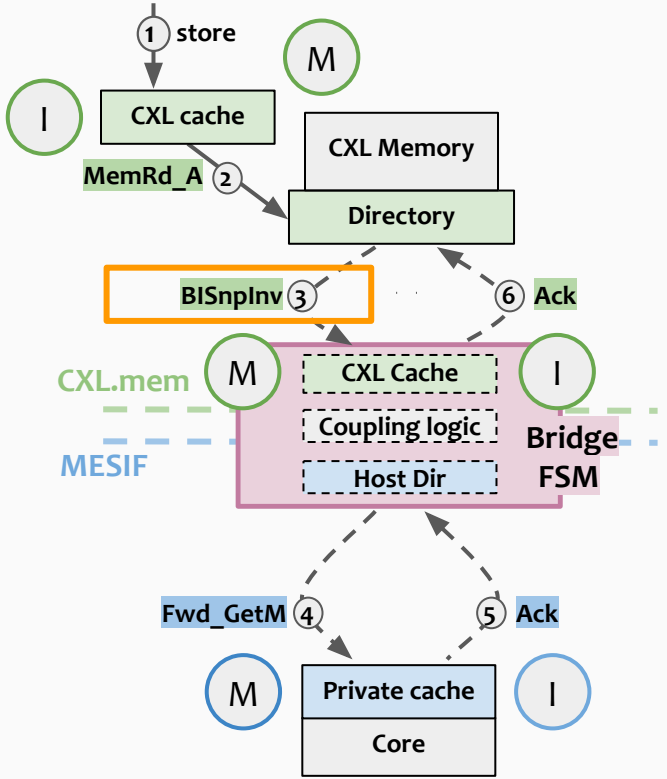

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How to generate the bridge FSM?

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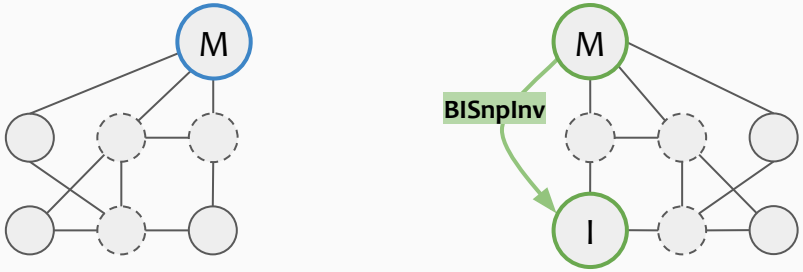
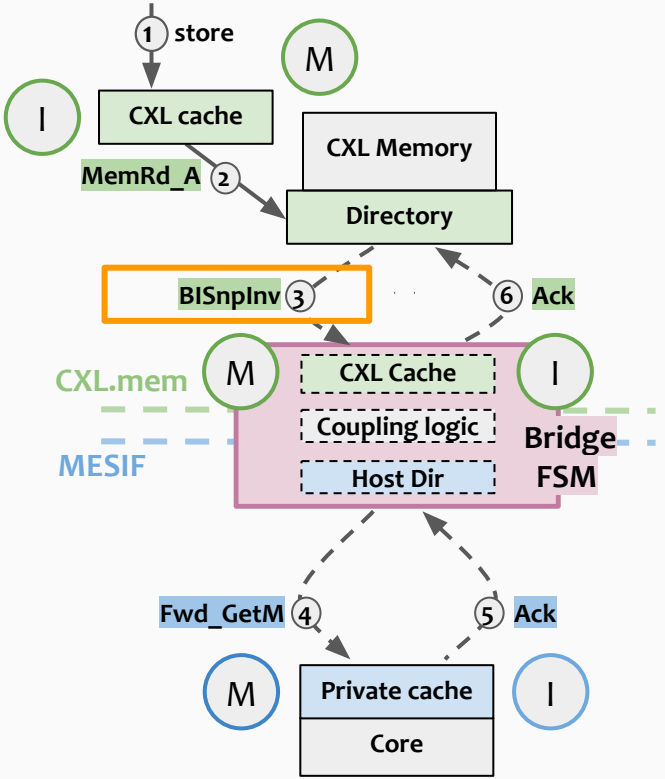


(cache permission downgrade)

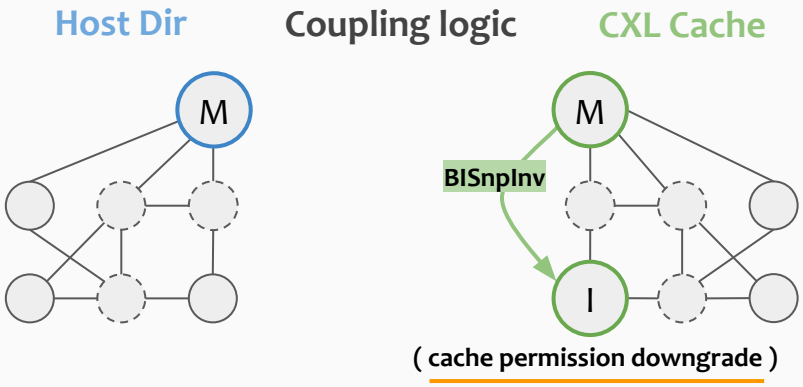
1. *Identify requests that must propagate*
2. *Deduce access of original requestor*



Synthesis: **Semantic translation**

How to generate the bridge FSM?

Static analysis of Host Dir & CXL Cache FSMs:



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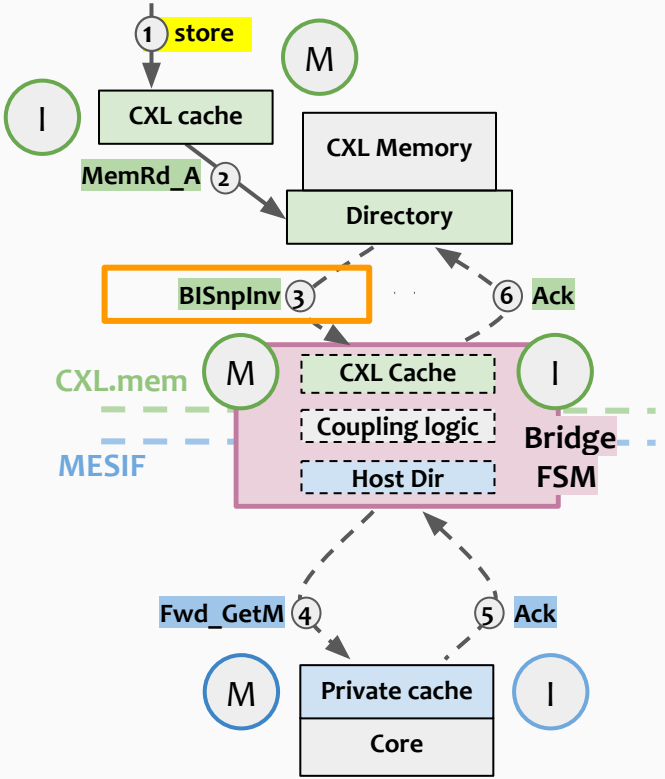
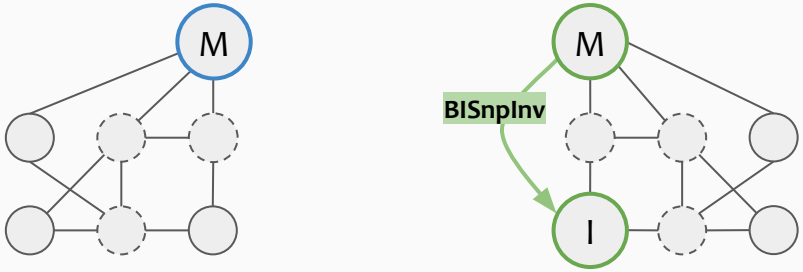


Synthesis: **Semantic translation**

How to generate the bridge FSM?

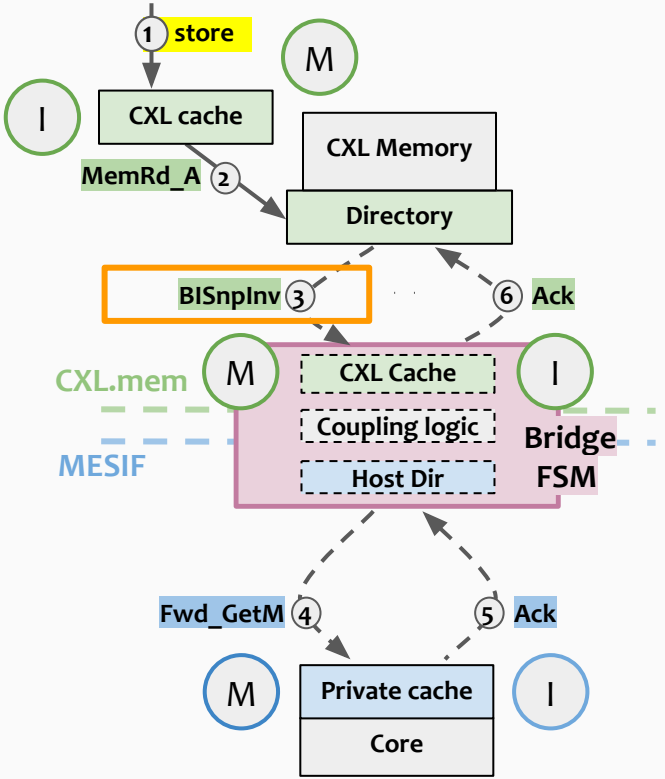
Static analysis of Host Dir & CXL Cache FSMs:

Host Dir | Coupling logic | CXL Cache



(cache permission downgrade)

1. *Identify requests that must propagate*
2. *Deduce access of original requestor*
3. *Simulate access to remote FSM*



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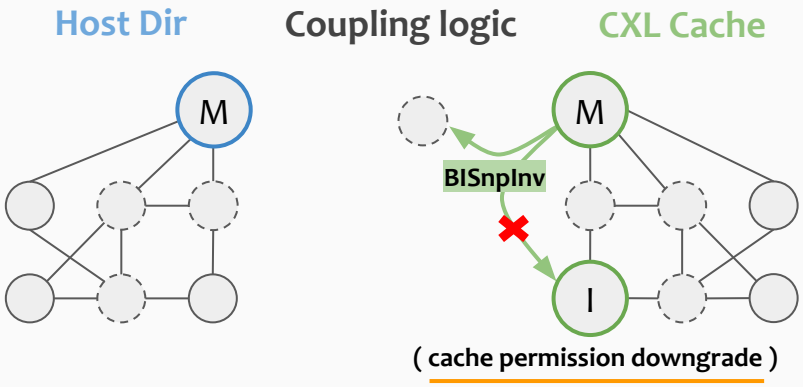
How to generate the bridge FSM?

Static analysis of Host Dir & CXL Cache FSMs:



1. *Identify requests that must propagate*
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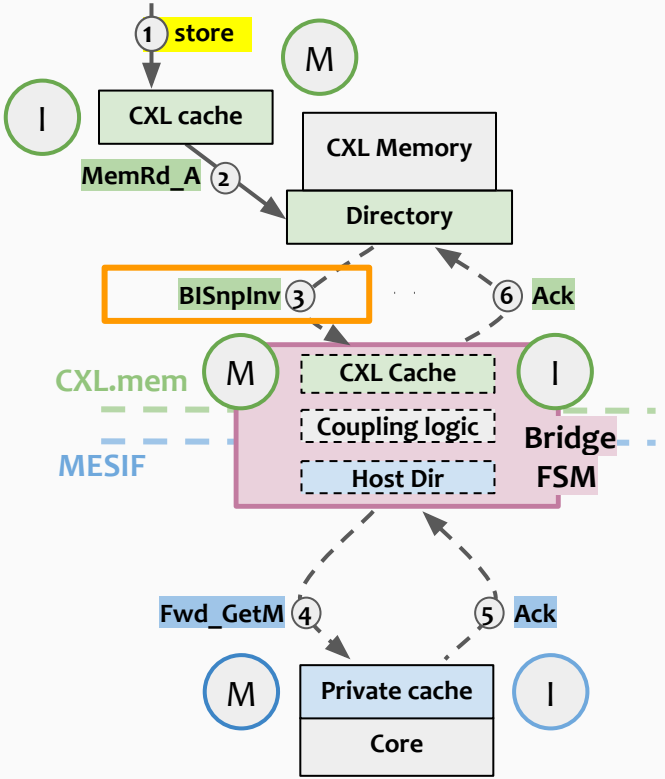

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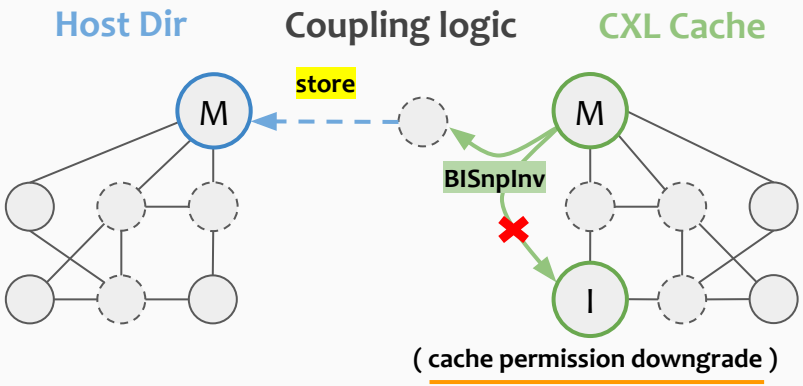
How to generate the bridge FSM?

Static analysis of Host Dir & CXL Cache FSMs:



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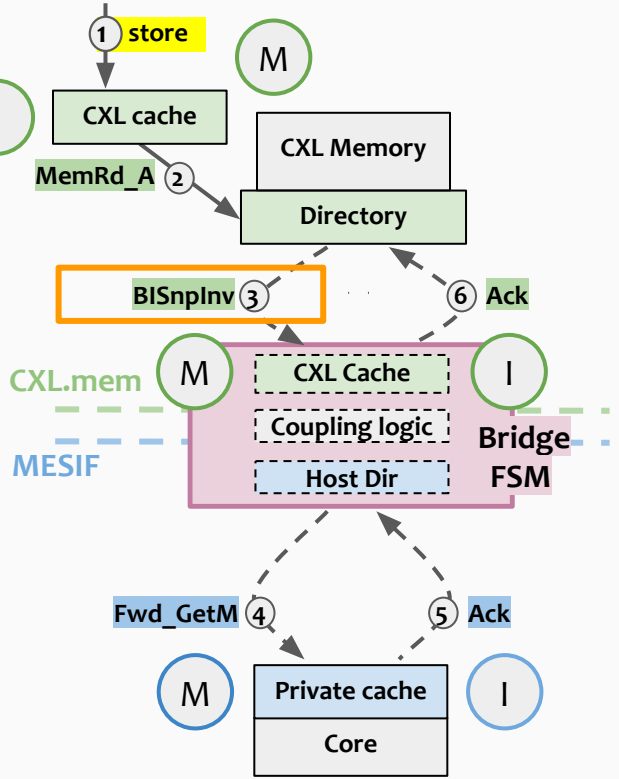

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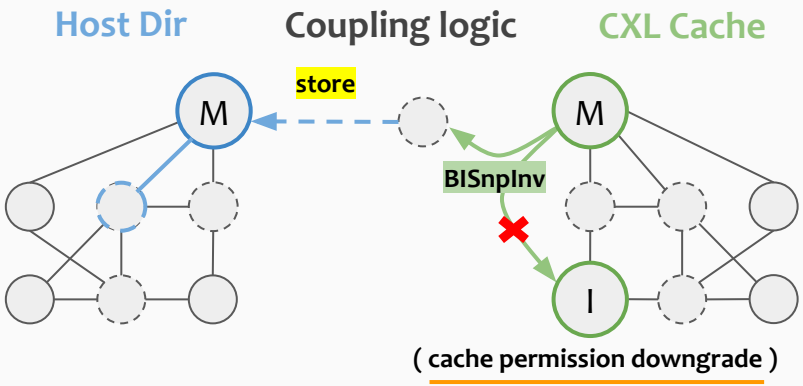
How to generate the bridge FSM?

Static analysis of Host Dir & CXL Cache FSMs:



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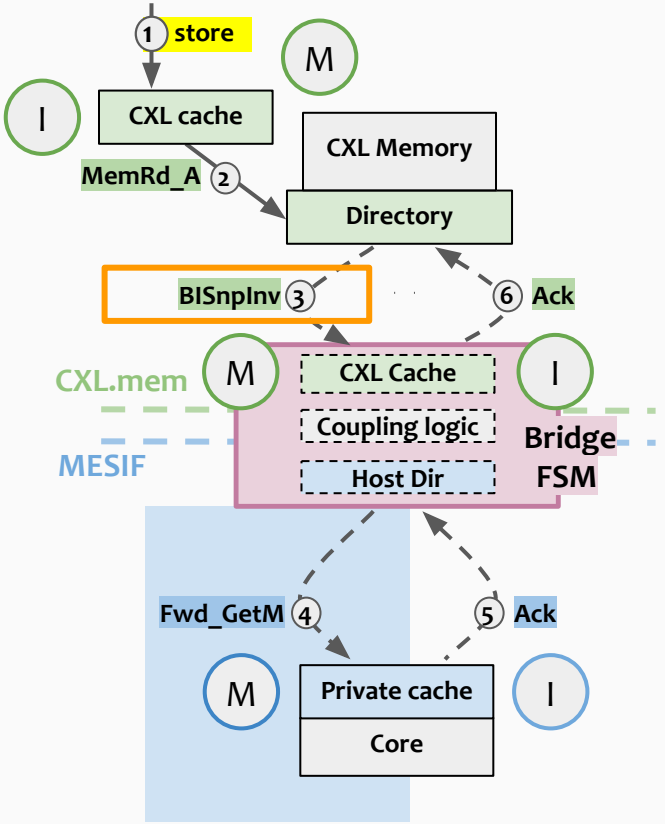
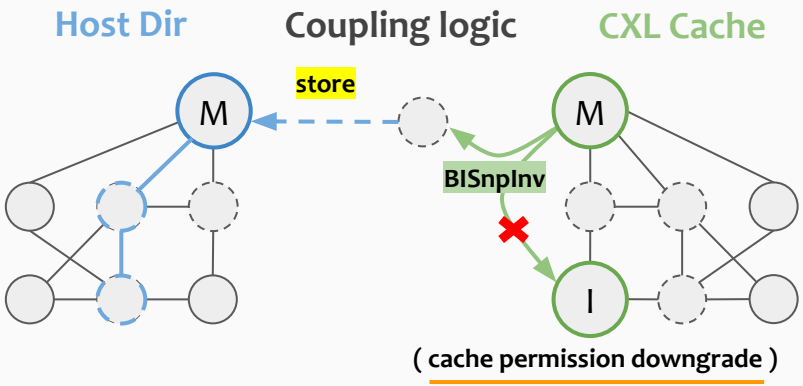


Synthesis: **Semantic translation**

How to generate the bridge FSM?

Static analysis of Host Dir & CXL Cache FSMs:



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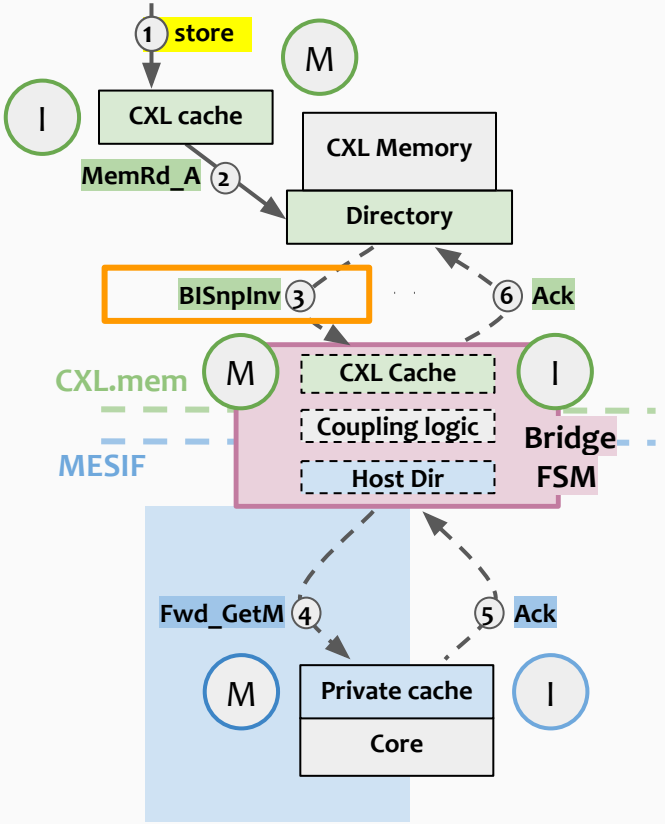

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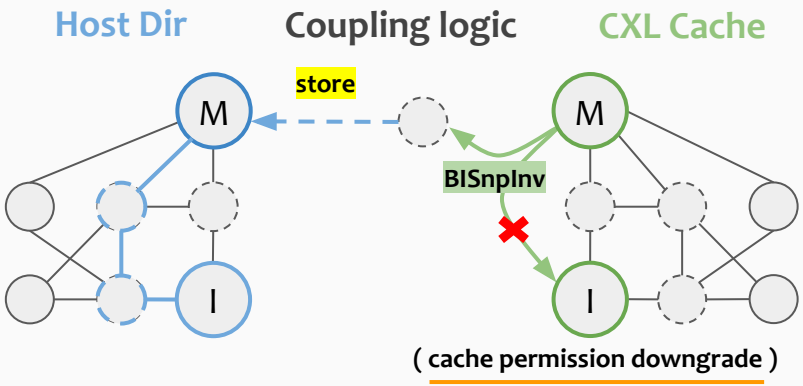
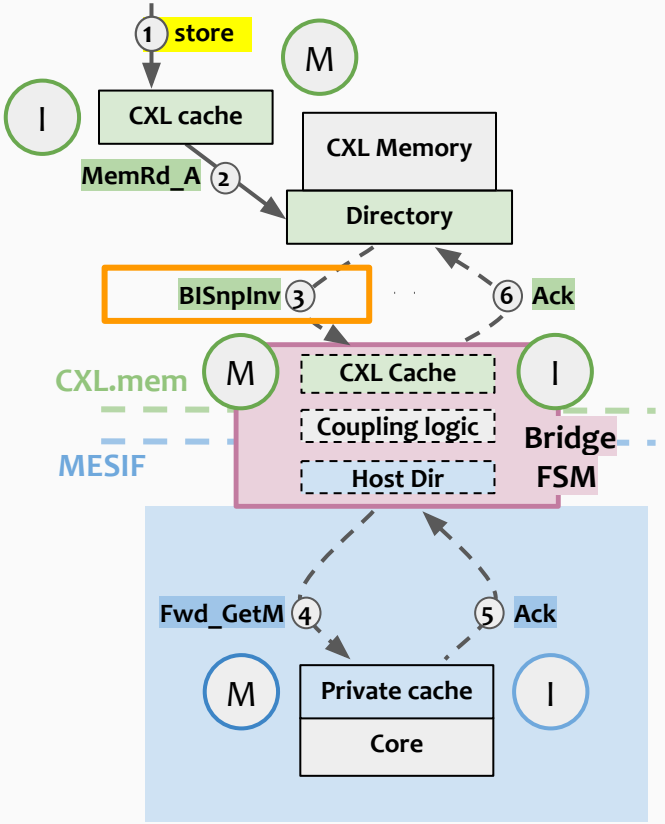
How to generate the bridge FSM?

Static analysis of Host Dir & CXL Cache FSMs:



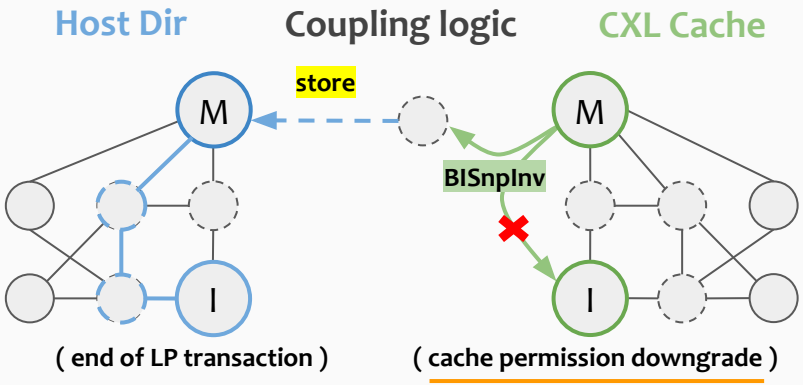
1. *Identify requests that must propagate*
2. *Deduce access of original requestor*
3. *Simulate access to remote FSM*



Synthesis: **Semantic translation**

How to generate the bridge FSM?

Static analysis of Host Dir & CXL Cache FSMs:



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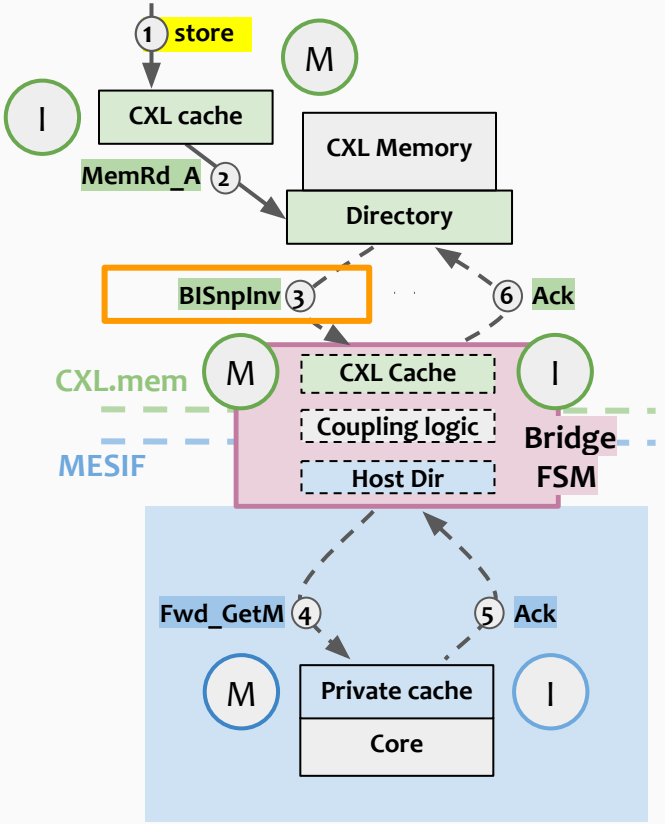
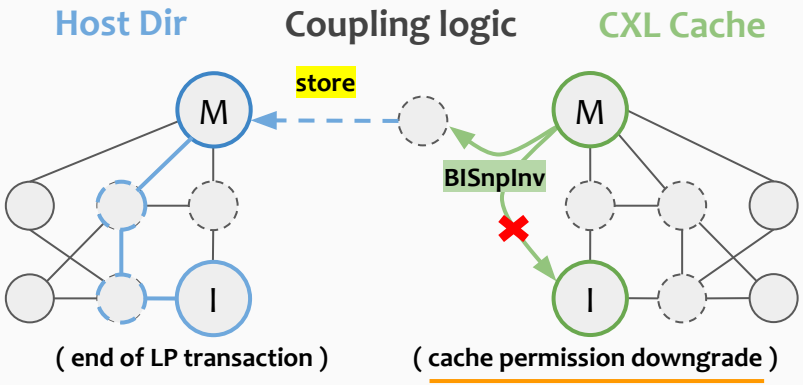
3. *Simulate access to remote FSM*



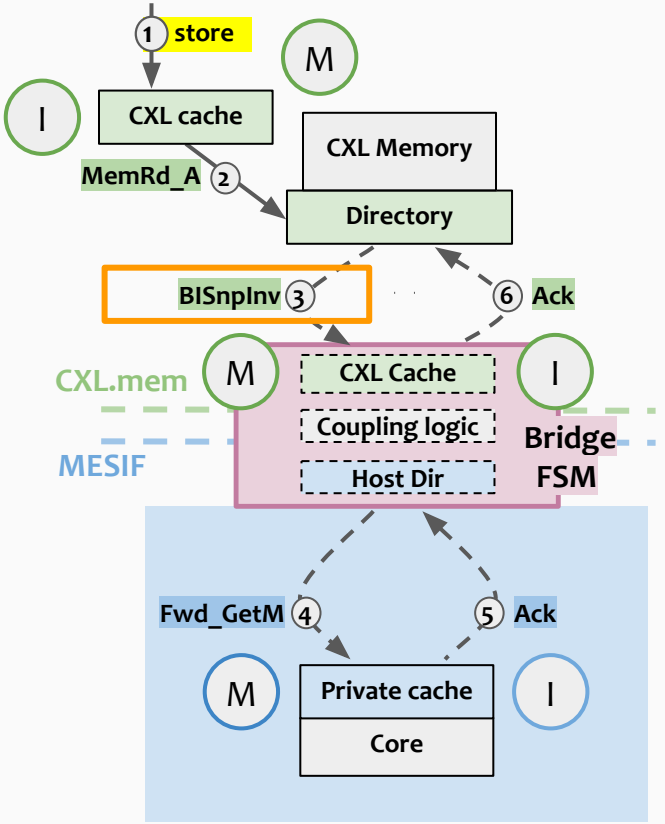
Synthesis: **Semantic translation**

How to generate the bridge FSM?

Static analysis of Host Dir & CXL Cache FSMs:



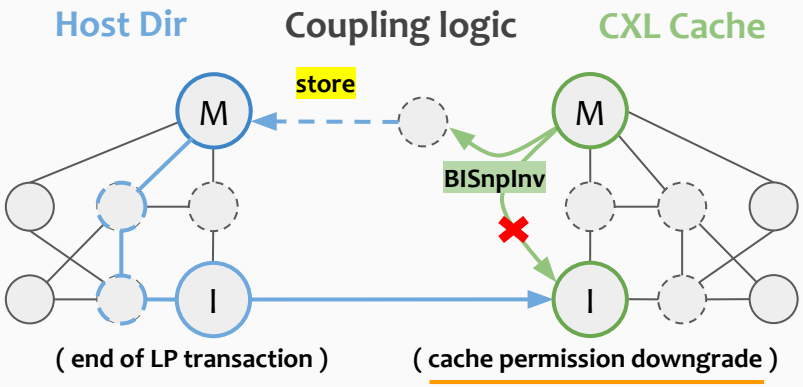
1. *Identify requests that must propagate*
2. *Deduce access of original requestor*
3. *Simulate access to remote FSM*
4. *Resume origin transaction*



Synthesis: **Semantic translation**

How to generate the bridge FSM?

Static analysis of Host Dir & CXL Cache FSMs:



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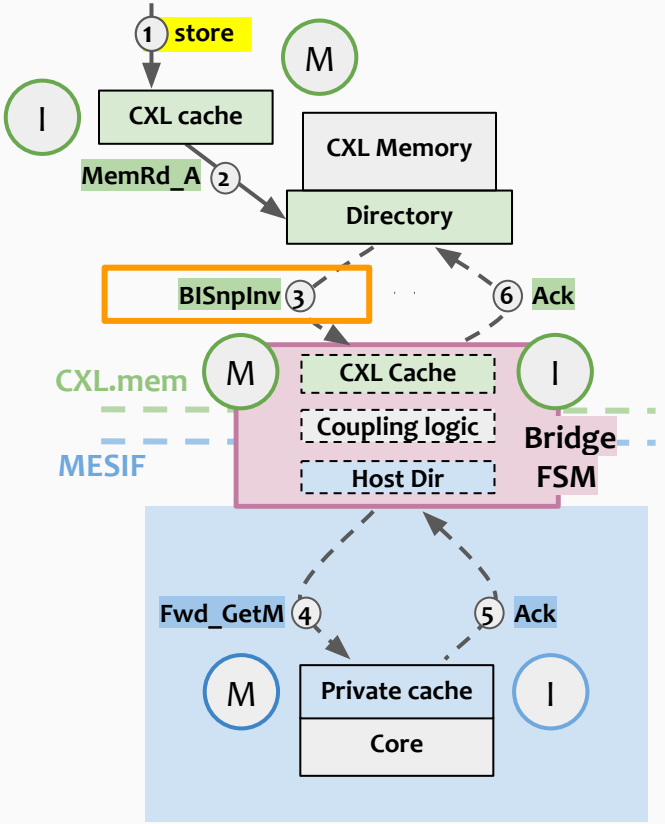

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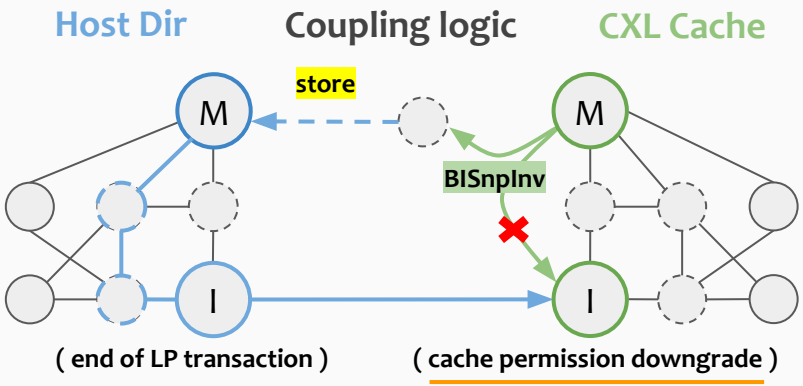

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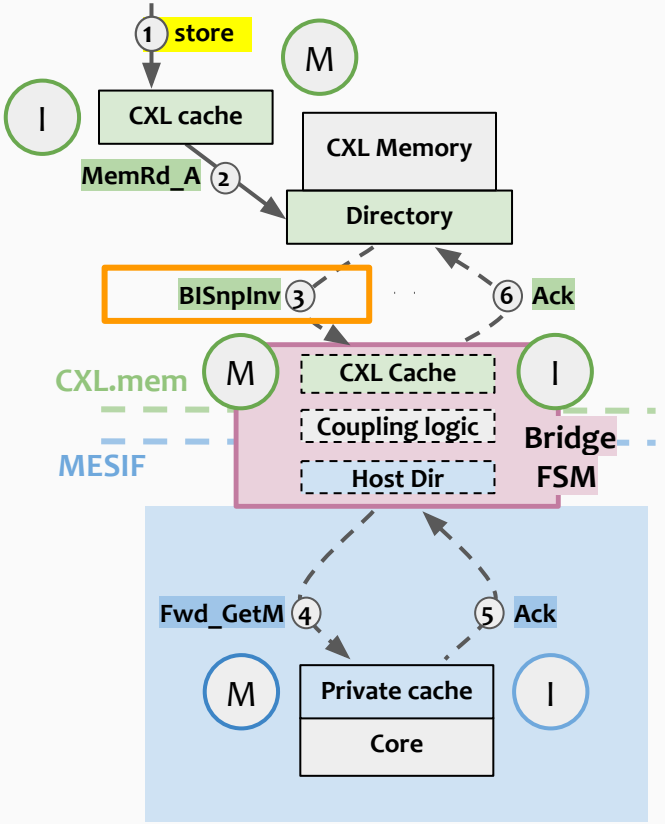

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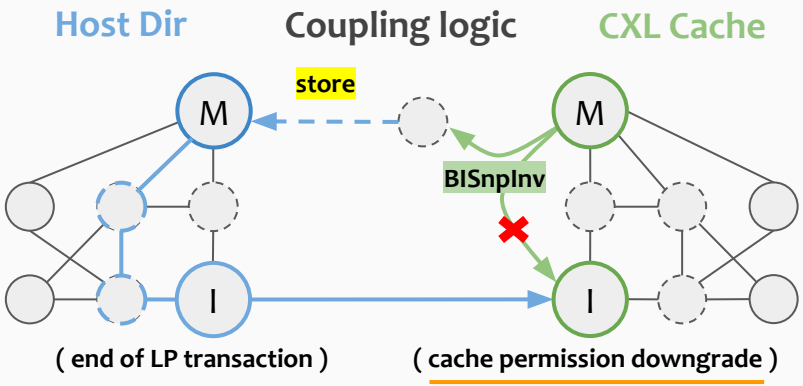

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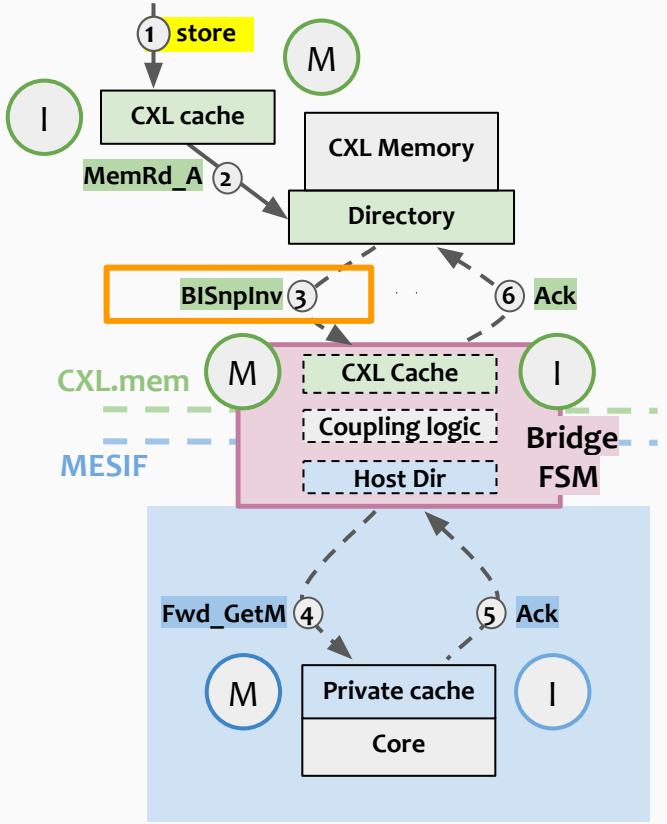

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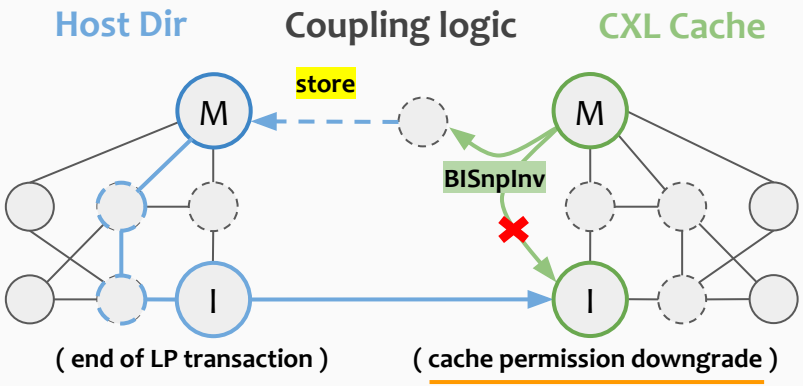

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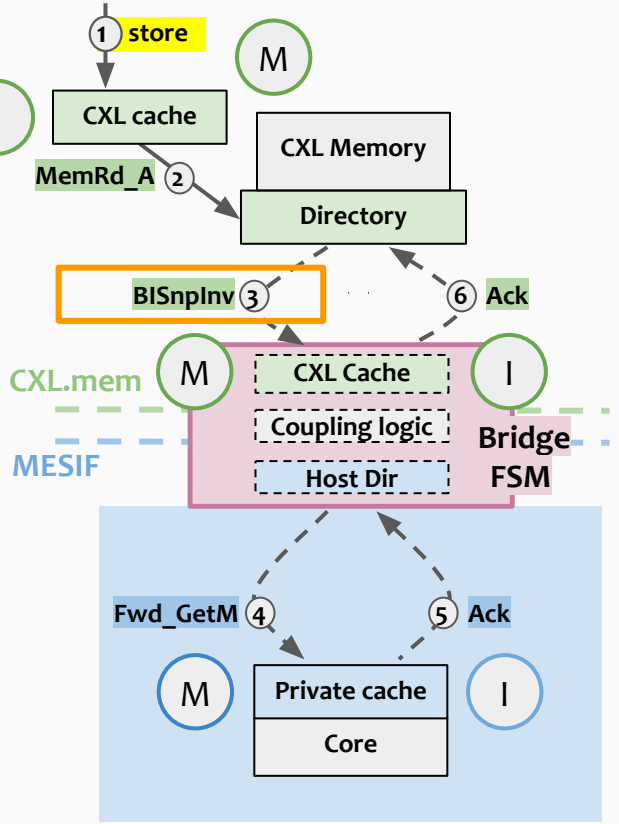

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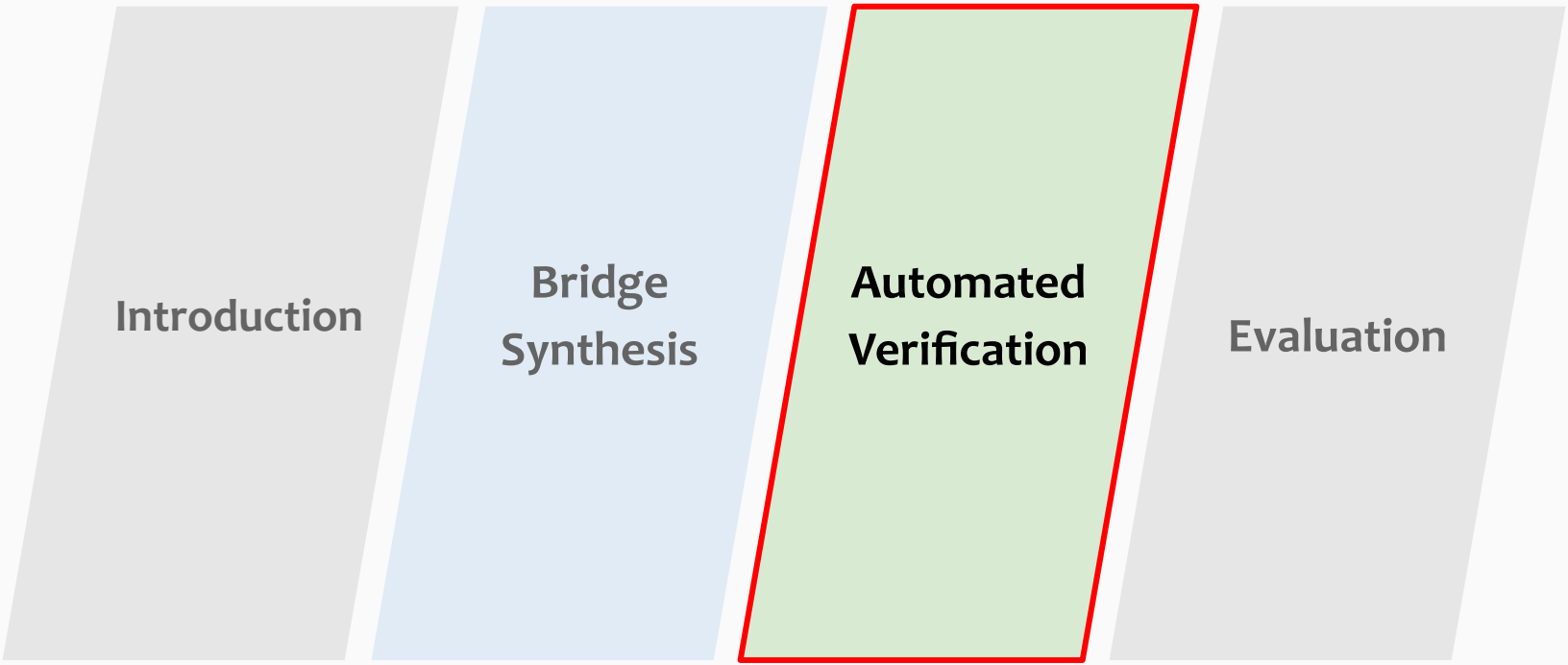
Introduction
Bridge Synthesis
Automated Verification
Evaluation

Verification: **Properties**

*Use **model checkers** to verify **heterogeneous** system models:*

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Safety

Adherence to Compound MCM

2

Liveness

Deadlock-freedom

All memory requests can terminate

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Compound MCM litmus tests[1]

Explore all litmus test instruction interleavings

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Liveness

Deadlock-freedom

All memory requests can terminate

Reachability of read/write permission state

Explore all possible instruction interleavings

[1] *Compound Memory Models*, Goens et al., PLDI'23

Verification: **Scalability**

Problem: *State space explosion of the liveness models*

Example:

Setup: MESI and RCC *clusters connected by CXL fabric*

Property: *Deadlock-freedom*

Configuration	Status	# of MC States	RAM usage
2 cores each	**Success**	22 Million	**12 GB**
3 cores each	**Out of Memory**	> 1.4 Billion	**> 1.8 TB**

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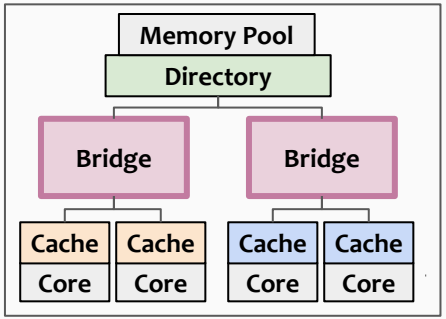
Full-system liveness models do not scale

Compositional verification

Idea: ***Compositional verification***

⇒ *Use multiple smaller models*



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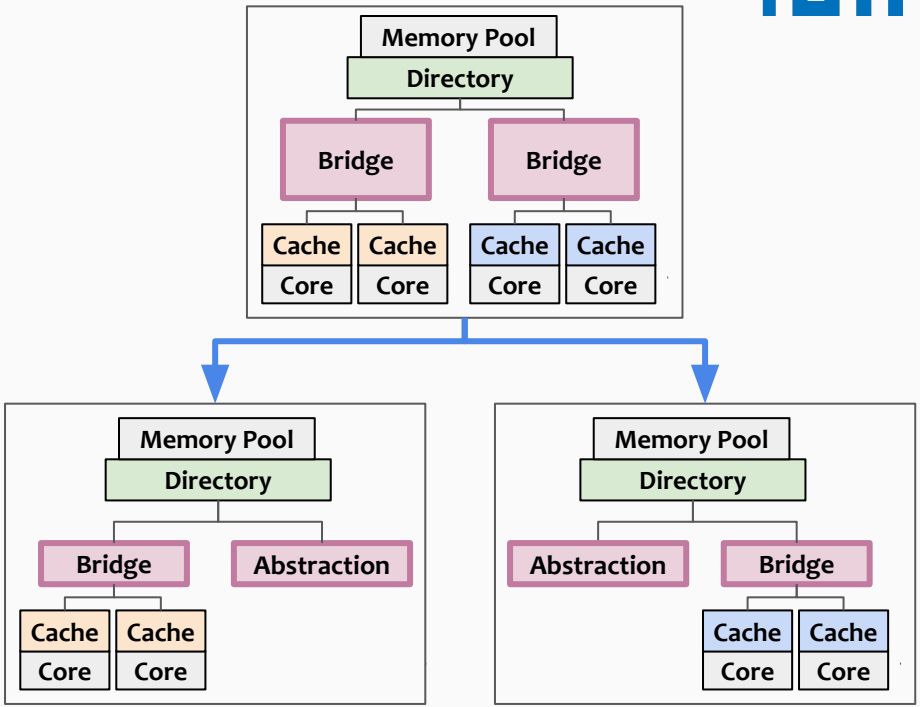

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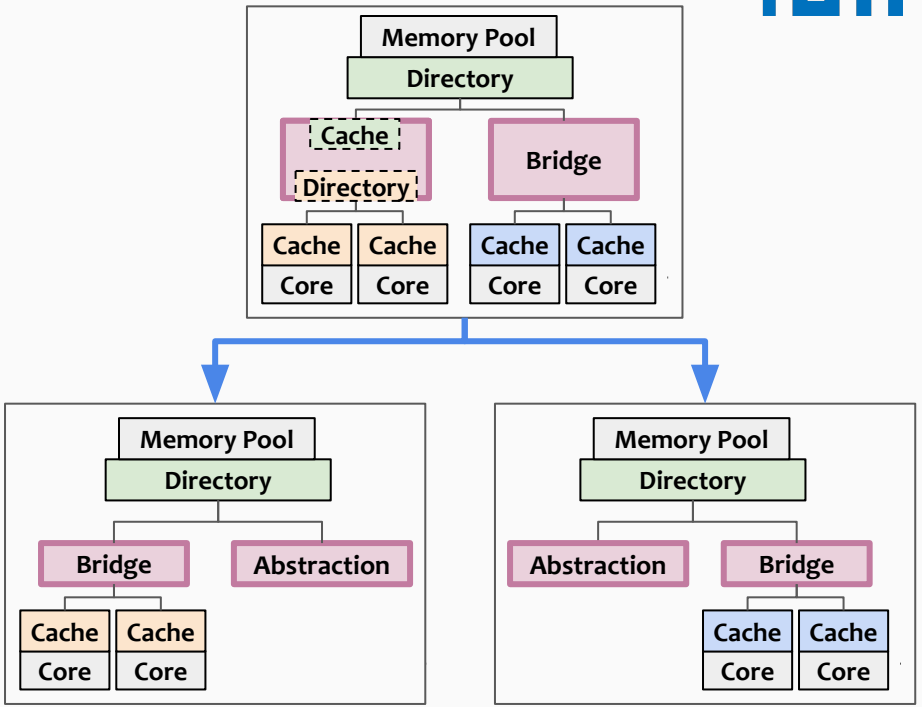
Bridge FSM is a fusion of cache and directory



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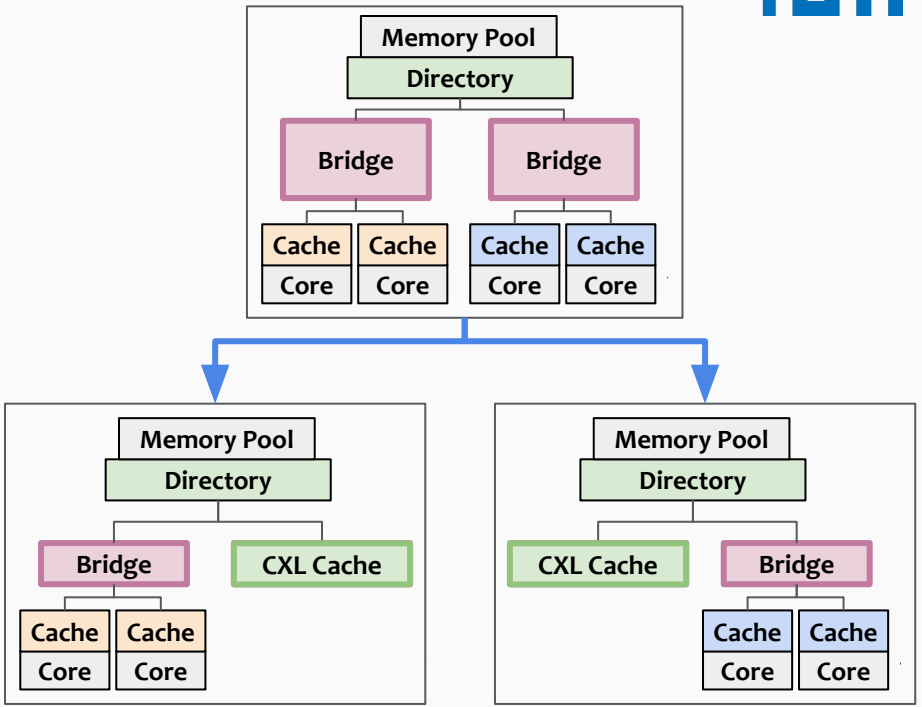

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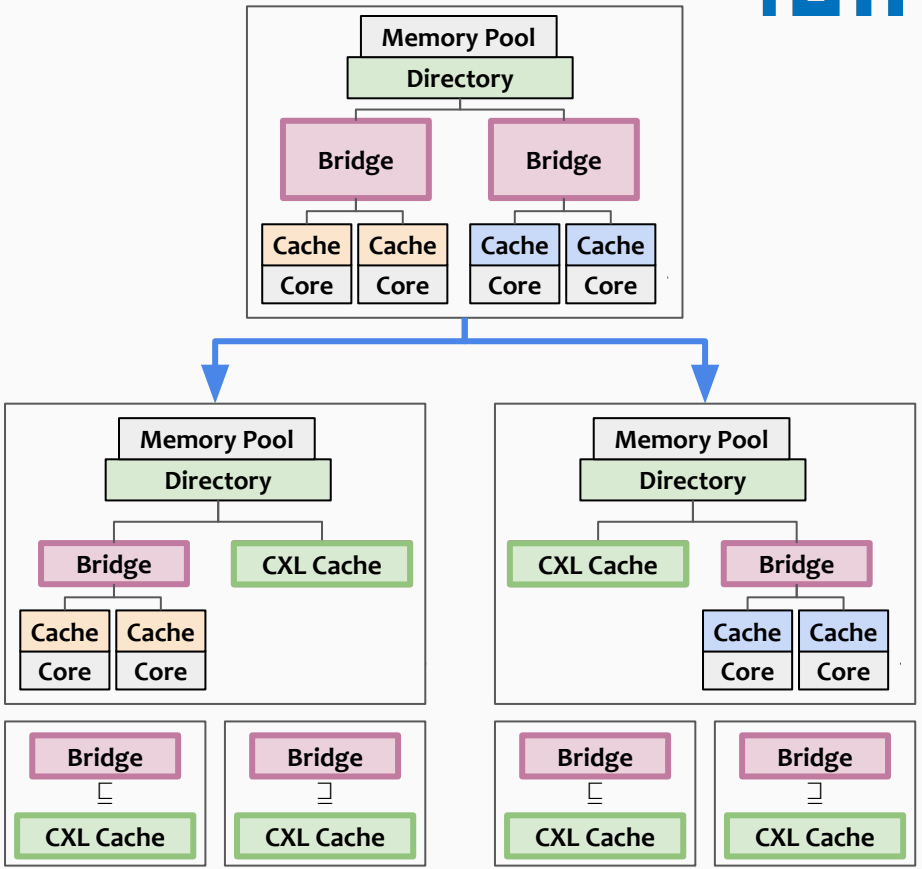
Abstraction Correctness:

Checked by additional models



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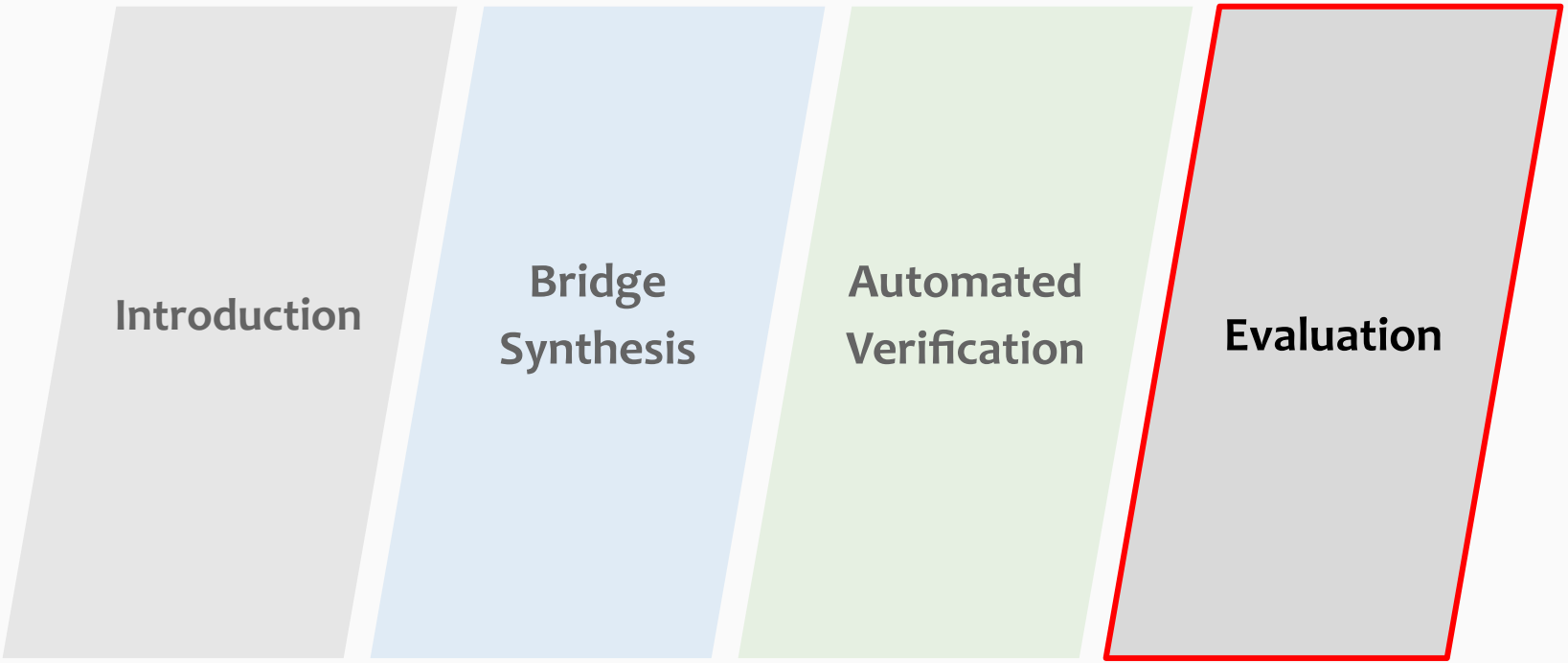
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Evaluation: **Goals**

1. **Correctness:**
   Verified safety + liveness using model checkers

2. **Generality:**
   Generated bridges for combinations of protocols:
   CXL, MSI, MESI, MOESI, RCC, RCC-O

3. **Extensibility:**
   Protocols are specified in a few hundred lines:
   CXL ⇒ ~650 SLOC, MESI ⇒ ~350 SLOC, RCC ⇒ ~200 SLOC

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4. How do the generated **bridges** affect **performance**?

5. Do **Compositional Verification** models improve **scalability**?

Performance evaluation: **Methodology**

Simulate system in gem5:

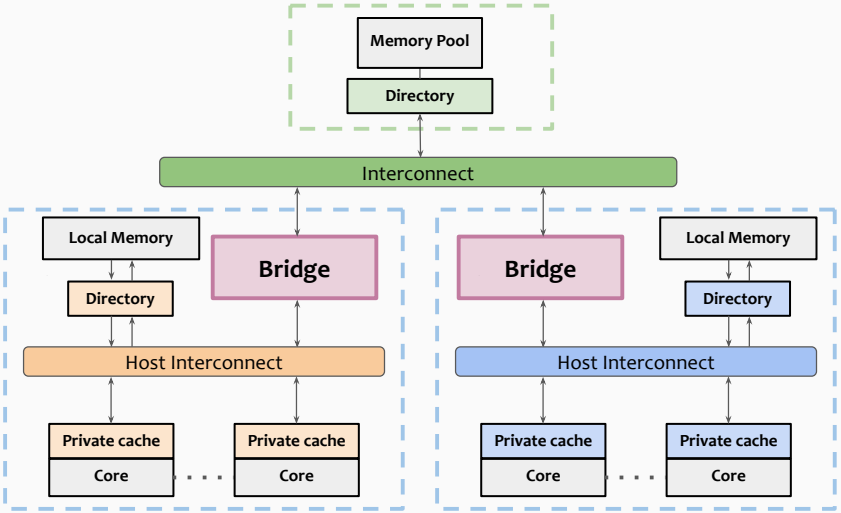
2 host clusters connected to remote memory

Hierarchical setups:

- **MOESI** (gem5)**:** Homogeneous with no bridge
- **MESI-Br:** Homogeneous with vCXLGen bridge
- **CXL-Br:** Heterogeneous with vCXLGen bridge

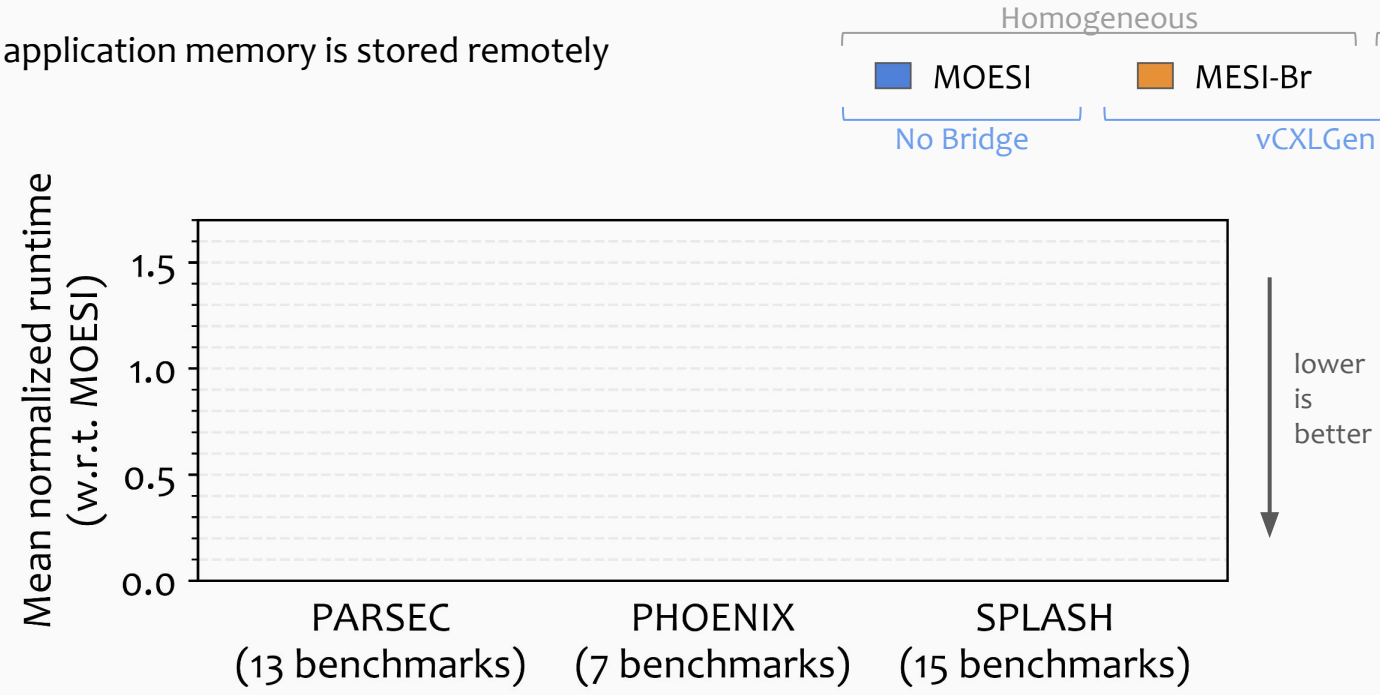
Evaluated scenarios:

1. **Worst-case:** All memory is stored remotely
2. **Distributed KVS:** Only shared memory is stored remotely



Performance evaluation: **Worst-case overhead**

Setup: All application memory is stored remotely



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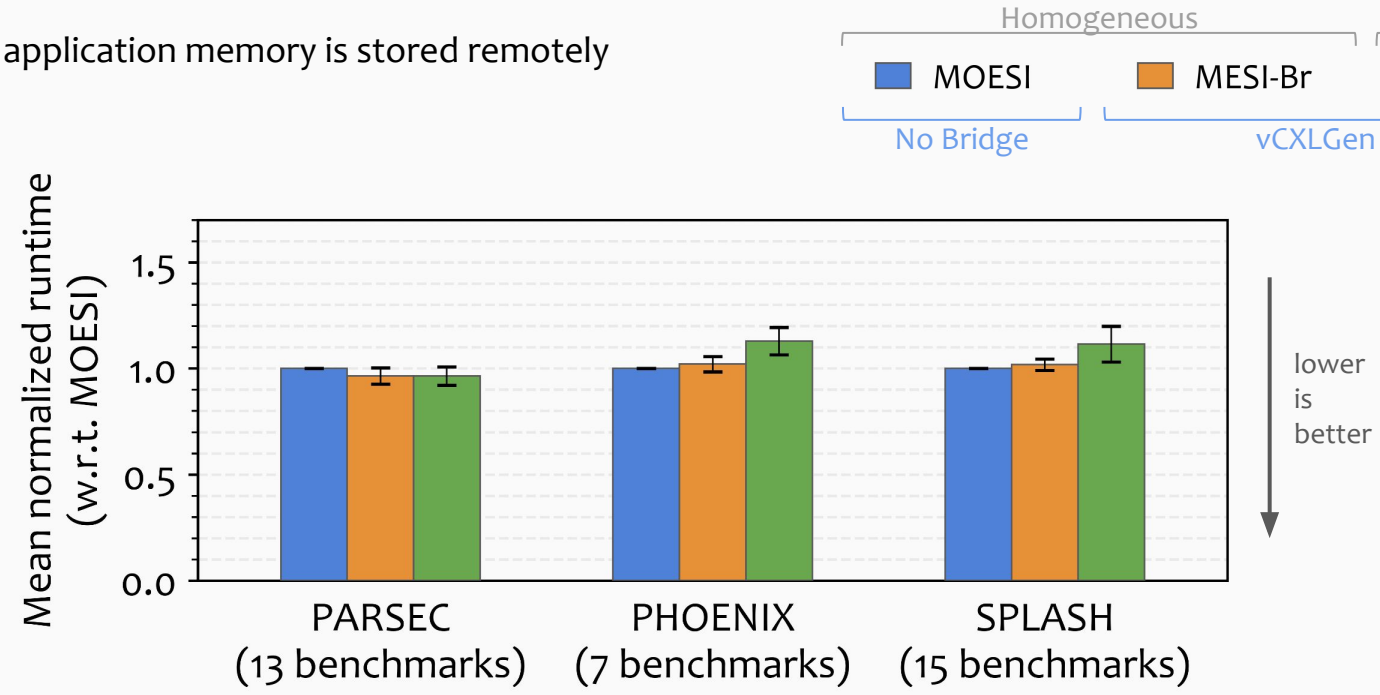

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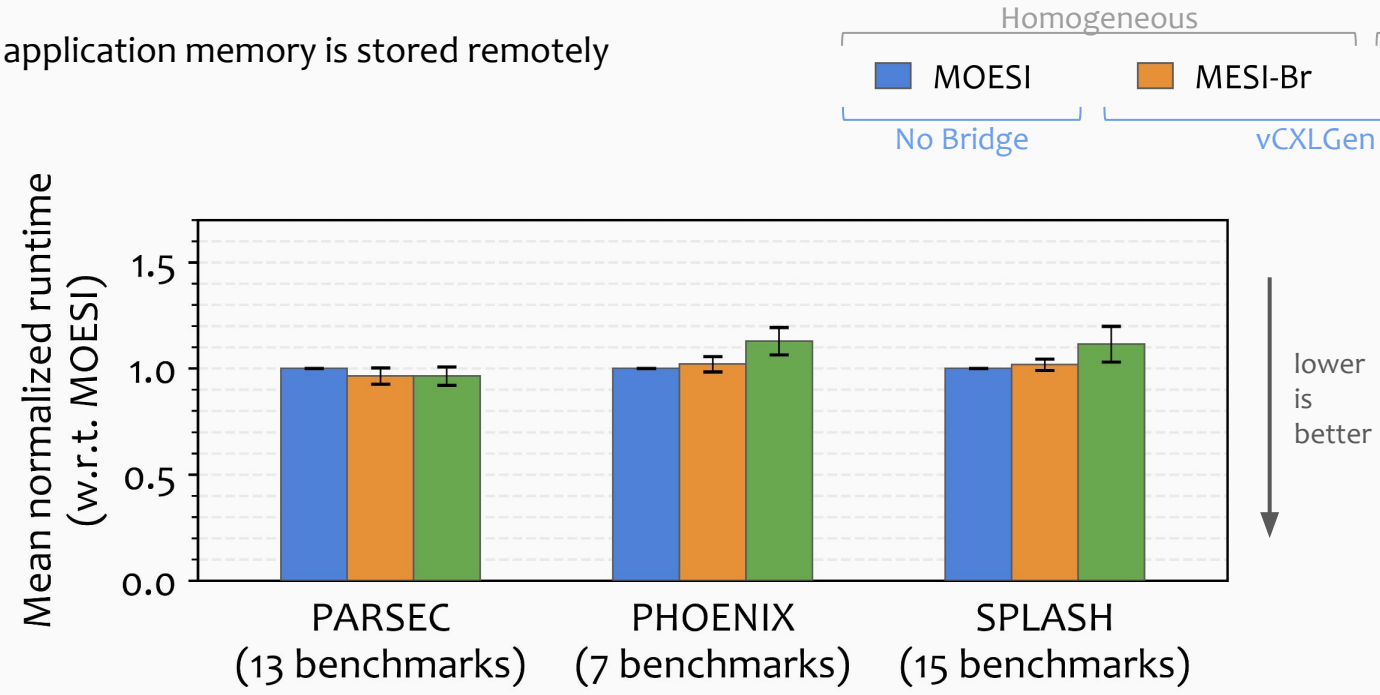
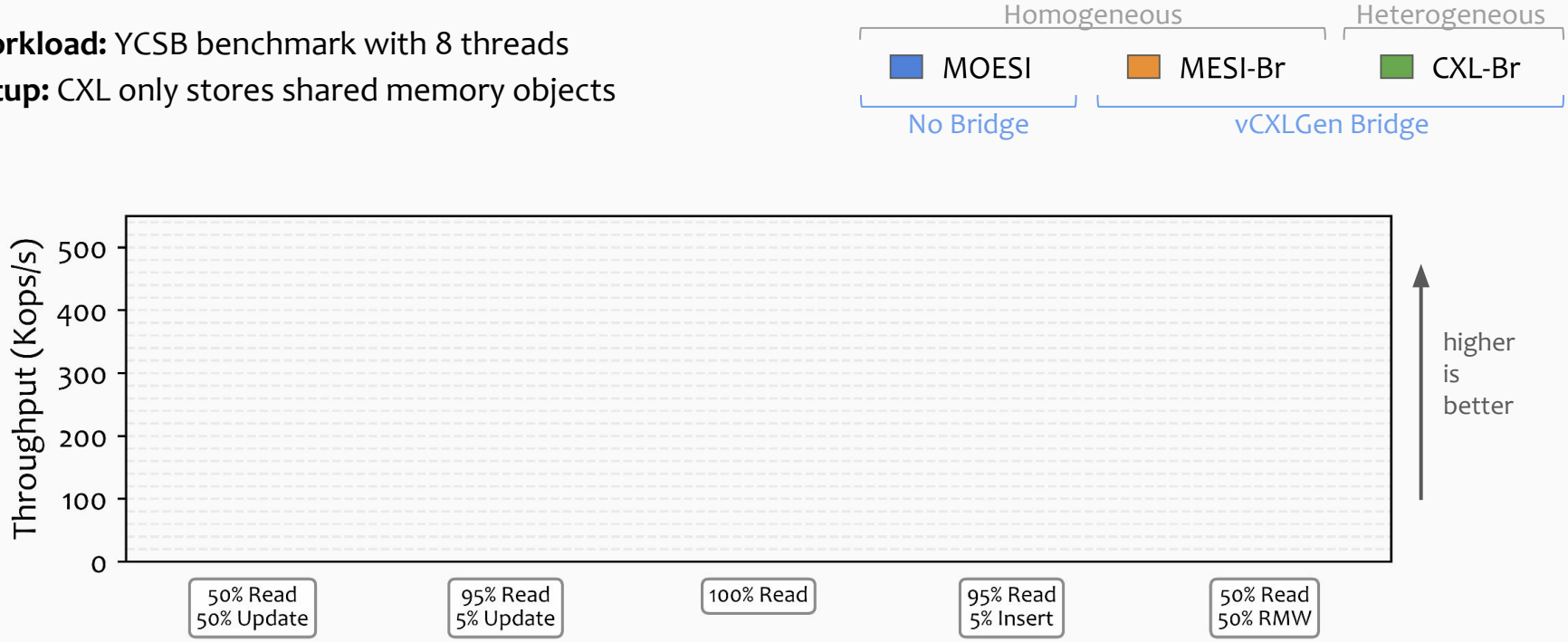


Takeaway: vCXLGen bridges perform **comparably** to a **homogeneous hierarchical MOESI** setup

Performance evaluation: **Distributed KVS**

Workload: YCSB benchmark with 8 threads

Setup: CXL only stores shared memory objects



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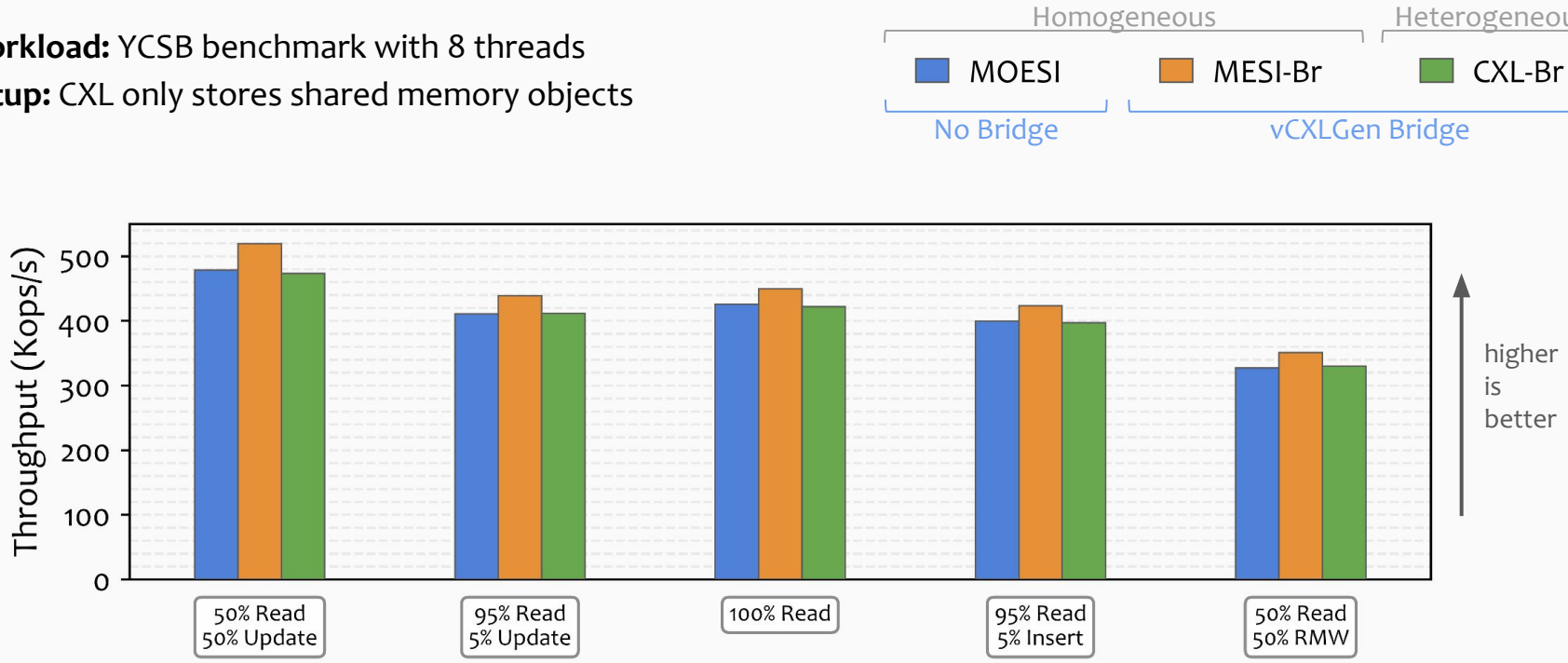

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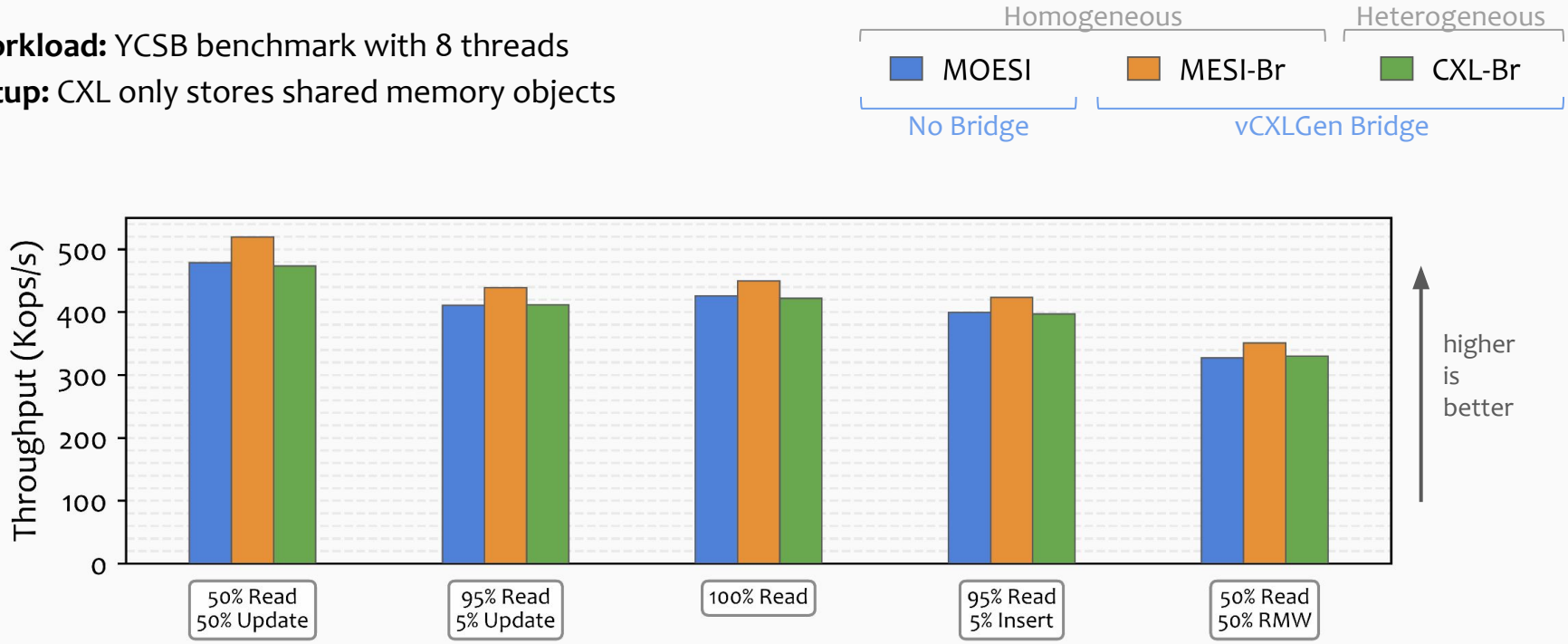
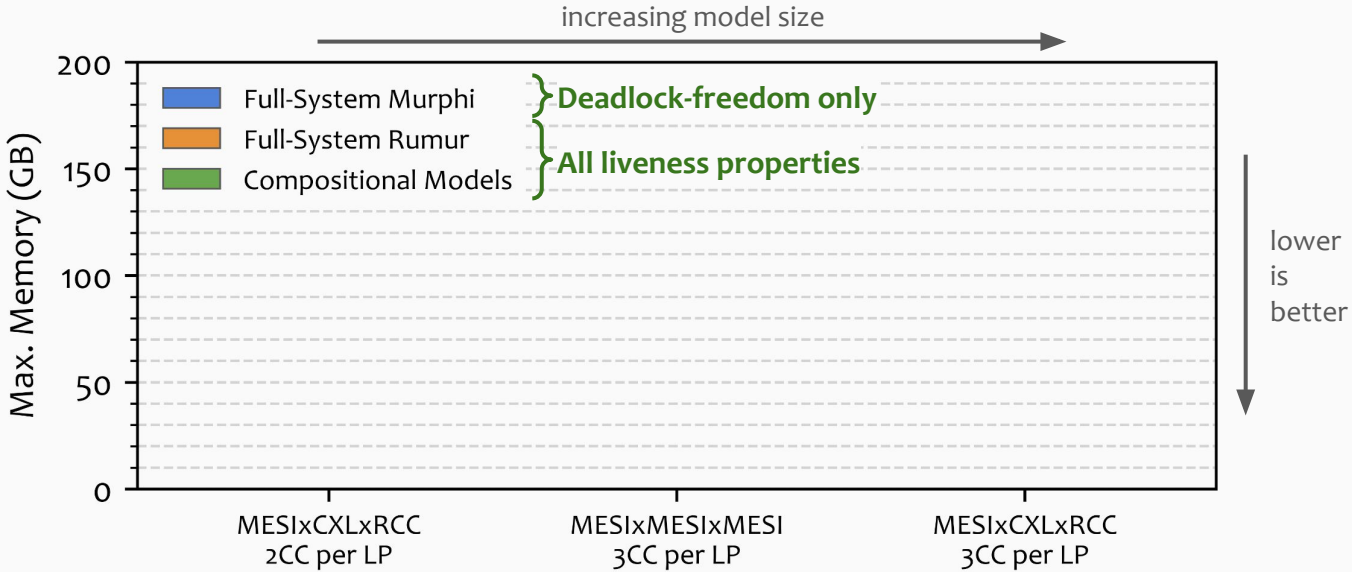


Takeaway: vCXLGen-generated bridges **preserve** the **performance** of real-world applications

Evaluation: **Verification scalability**

Do vCXLGen's compositional models use less memory?



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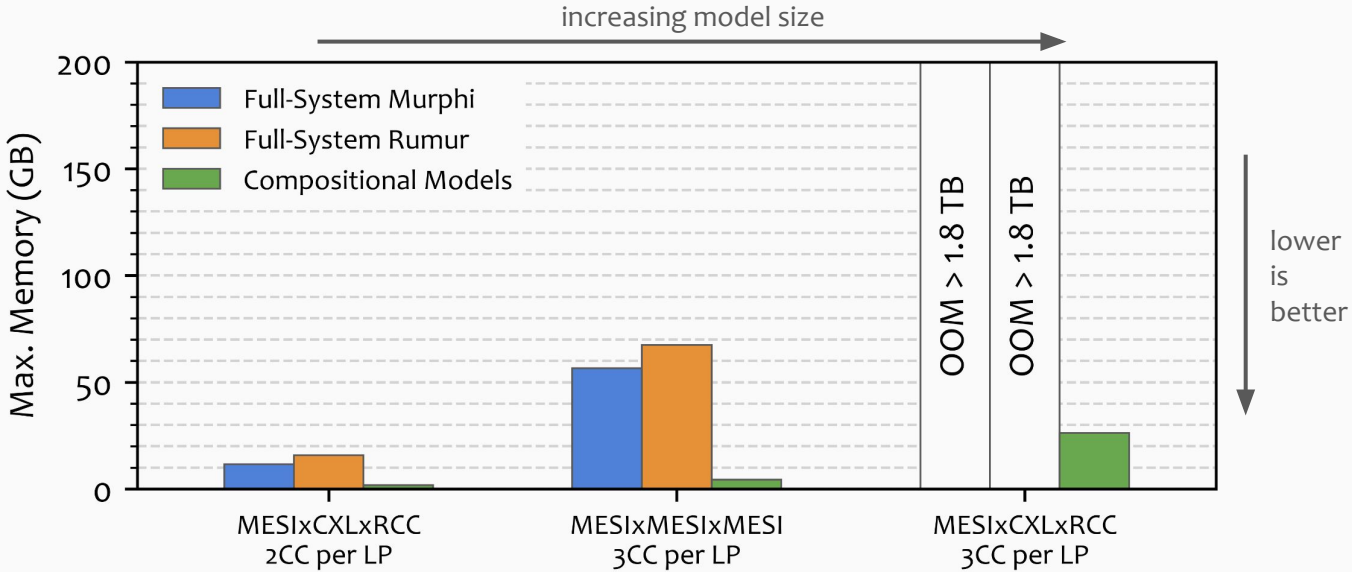

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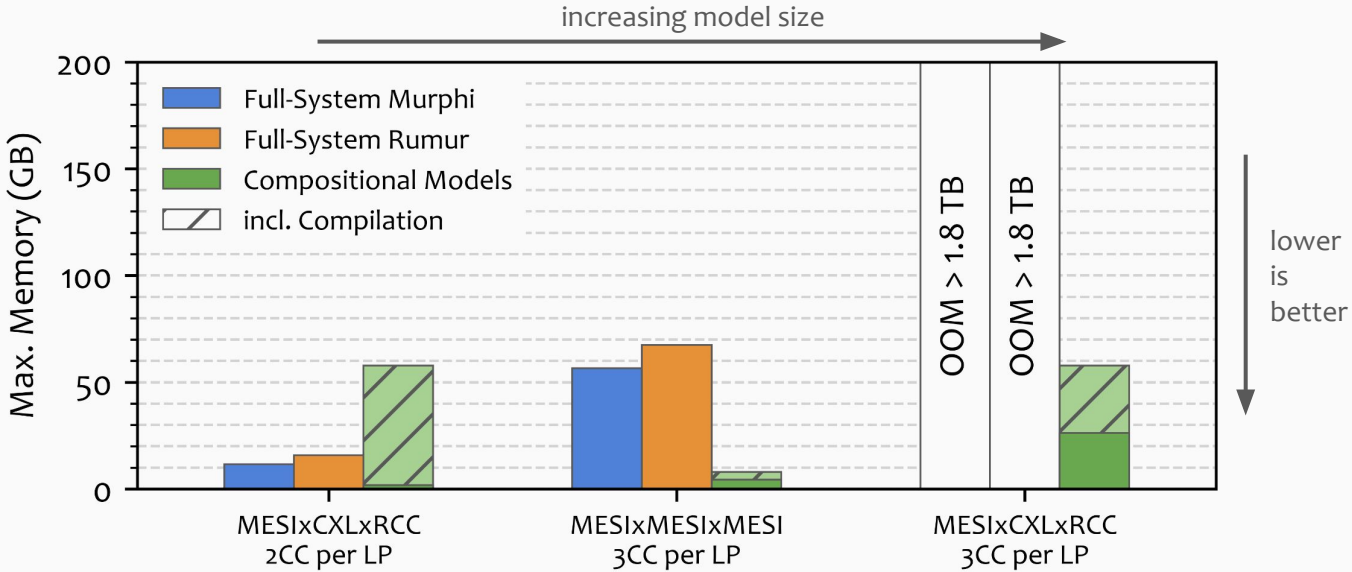

Observation: *Compilation depends on model complexity*

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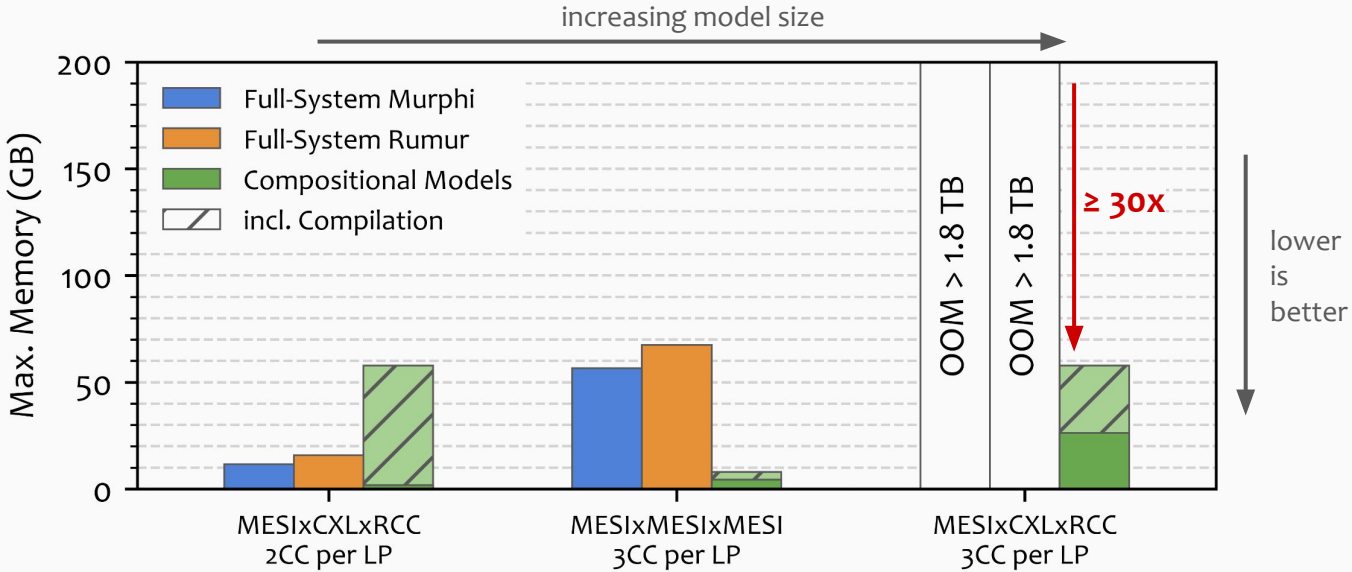


Observation: *Compilation depends on model complexity*

Takeaway: Compositional models enable the **verification of larger systems** with **less memory**

Conclusion

Motivation: Current CXL hardware does not support heterogeneous architectures

Problem: How to **automatically** and **correctly** extend heterogeneous architectures for CXL memory?

Solution: vCXLGen — Synthesize *verified* CXL coherence bridges from protocol specifications, that **translate** host protocols to **CXL.mem** & preserve original semantics of heterogeneous architectures

vCXLGen key ideas:

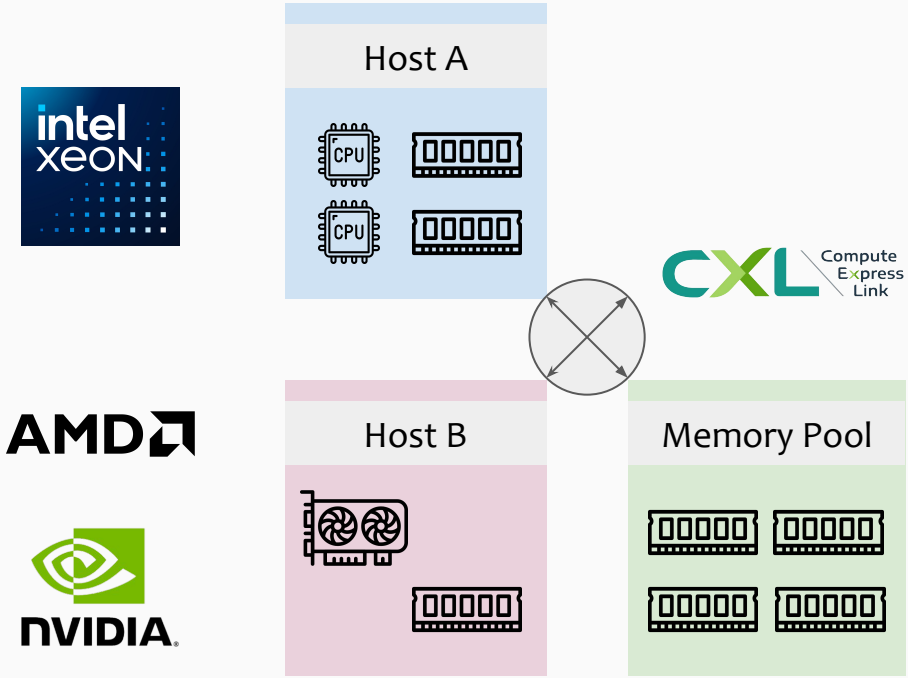
- **Compound State Machine:** combine FSMs of host directory & CXL cache
- **Protocol Semantic Translation:** statically detect *propagation* & *translation* with CXL.mem
- **Compositional Verification:** leverage the bridge's construction principle to decompose verification models

Open problems:

- **Accelerator integration (e.g., GPUs):** CPU-GPU symmetric coherence with CXL 3.0

What's next? Accelerators!

E.g., CPU ⟷ GPU **symmetric coherence** with **CXL 3.0**



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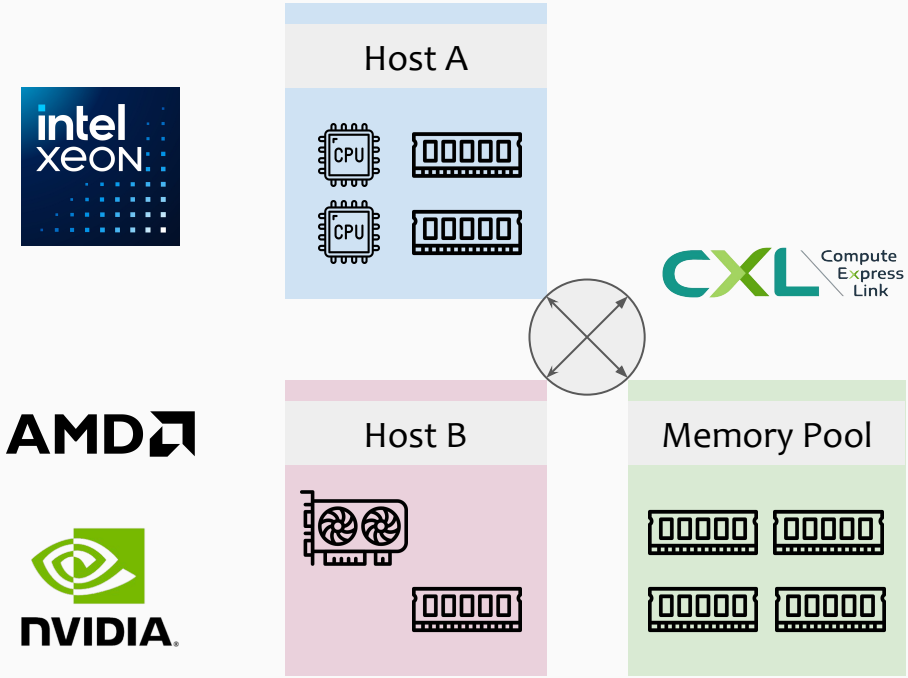

vCXLGen GPU Roadmap:

- ✅ Release-consistency GPU MCMs
- ✅ Update-based GPU protocols
- ✅ Write-through GPU protocols
- ⏳ **Scoped memory models:**

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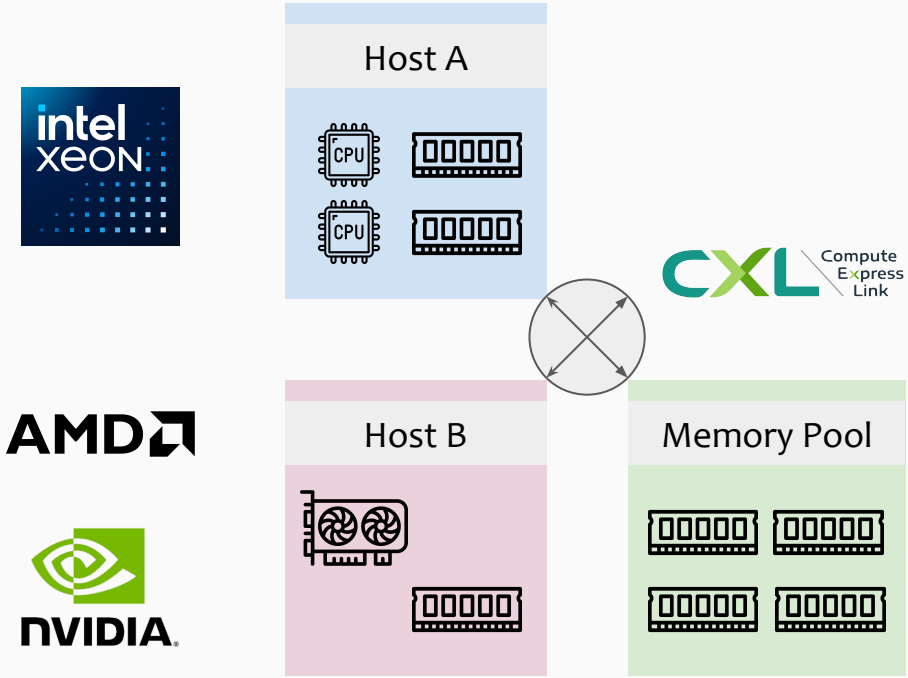

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- ✅ Update-based GPU protocols
- ✅ Write-through GPU protocols
- ⌛ **Scoped memory models:**
  - GPUs tag memory operations with a **coherence scope**
    [Block] [GPU] [System]

Backup slides